Analysis of Thermal Vias in High Density Interconnect Technology

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Abstract

An analytical approach is presented for the thermal modeling of via networks used in removing heat from chips in high density multichip module designs. The routing density available to the electrical design engineer is directly affected by the presence of thermal vias. Achieving a balance between optimum thermal performance and electrical design flexibility is therefore of considerable importance.

The thermal resistances of the components making up a typical via network cell are accurately determined by the closed form expressions. The complete thermal resistance between the die and substrate can be henceforth determined by constructing the unit cells in a combination of series and parallel paths, allowing for the thermal spreading effect through the via network, and the epoxy and planarizing layer thermal resistances. Computed predictions are compared with numerical and experimental results, and good agreement was achieved using an accurate yet simple methodology.

Introduction

Heat removed from a microelectronic chip located within a package module is a subject of serious concern in the industry as a result of increasing circuit density, hence operating power levels. Enhancing thermal performance means reducing the die operating temperature, and this can be achieved by several current approaches [1] which may be lumped into two categories:

External Enhancement:

i) enhanced convection cooling
ii) heat sink attachment

Internal Enhancement:

iii) microchannel cooling
iv) die interconnect technology
v) optimal package material selection

External enhancement techniques can indeed provide tremendous reduction of temperatures, and this is largely controlled by whether the system is operating under natural convection or forced convection conditions, liquid or air ambient media, and the density of the circuit boards containing the packages (i.e. heat sources) in the system. Heat sinks provide for optimal surface area enhancement, but there is a limit to their effectiveness since the package heat flow path may not be directly in line with the attachment location [2].

Internal enhancement aims at either cooling the chip locally or decreasing the package resistance. In microchannels, removal is redirected to another ambient condition. By decreasing the package resistance, that is, the junction-to-case or junction-to-board thermal resistances, the heat flow increases to the existing package surfaces, hence decreasing the die temperature. Using alternative package material with higher thermal conductivity, heat flow can be enhanced to the external surfaces. However there exists a practical tradeoff with electrical interference and thermal conduction.

Recently, die interconnect technology has been examined whereby a percentage of electrical interconnect network (vias) are used for thermal transmission purposes [3,4]. This provides for enhanced direct heat removal from a die to a lower substrate zone which is closer, or at, the external surface or heat sink attachment interface. Recent multichip technology [5] has been incorporating these thermal via networks.

In this study, closed-form analyses are carried out on staggered type thermal via networks, typically of copper-polyamide construction. The via networks are located beneath the die on spaced, island-array patterns. The space between these islands makes up the typical zone that is available for electrical routing interconnections. Thermal resistances are evaluated for islands of thermal vias and the results are compared to recently published data obtained for a typical thermal test substrate with staggered via networks [3,4].

In addition to a detailed description of the development of the present model, comparisons of the predictions with experimental results are presented. Also, studies are carried out comparing the effectiveness of using various thermal enhancement options, such as thermal vias, thermal wells, and partial thermal wells (see Fig. 1). The effects of percentage routing densities, planarizing layer, and effective thermal conductivities are examined as well.

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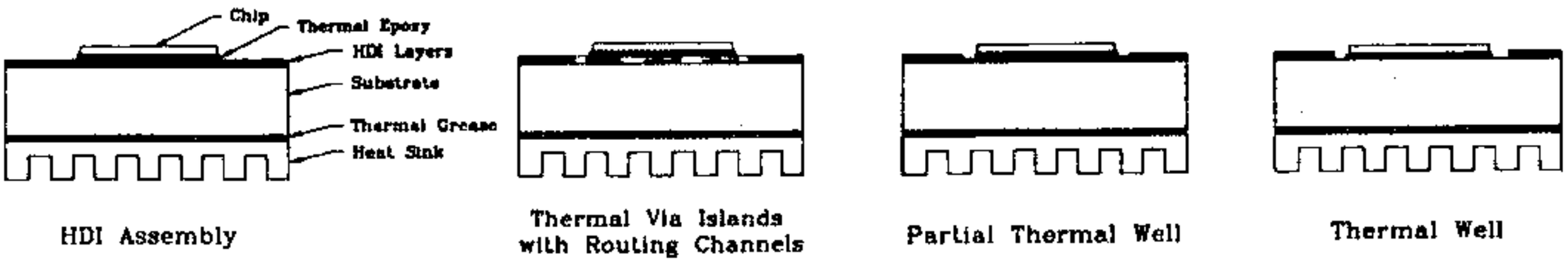

Figure 1: Typical configuration of high density interconnect assembly and thermal enhancement options

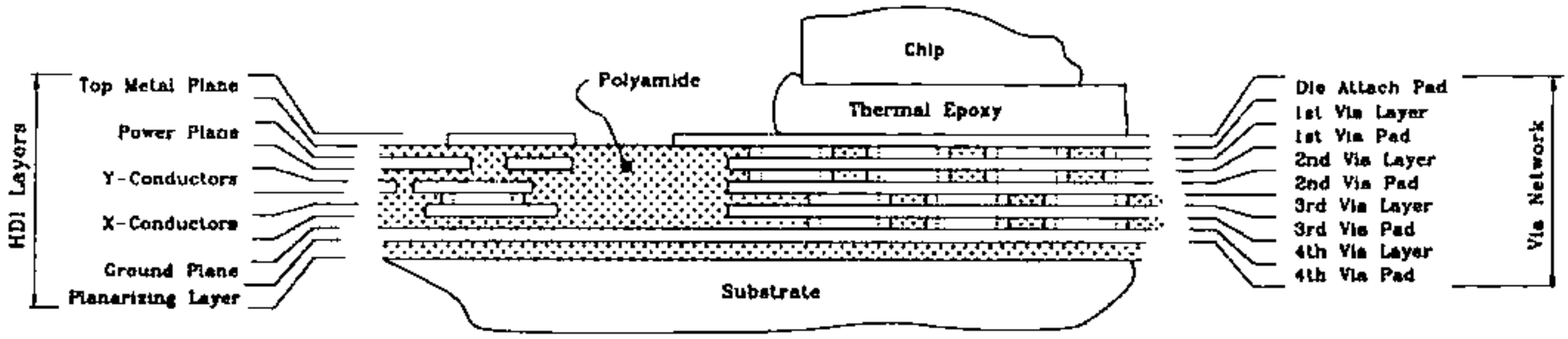

Figure 2: Typical 5-layer high density interconnect routing configuration shown with 4-layer via network

Thermal Modeling

Via Networks

Figure 2 depicts the typical configuration of a 5-layer High Density Interconnect (HDI). It consists of 5 conductive layers alternately staggered with 5 polyamide dielectric layers. In this study, conductive and polyamide layers are 5μm thick and a typical 5-layer HDI, shown in the figure is therefore 50μm thick from the top metal plane to the top of the substrate. The top conductive layer, on which the die is attached using epoxy, is called the die attach pad and, in this study, is made of gold. The remaining conductive layers are made of copper. The bottom polyamide layer is called the planarizing layer and may be eliminated if the bottom conductive layer, the ground plane, contains no electrical signal lines.

In enhancing the thermal performance of HDI layers, the top of polyamide layer beneath the die may be removed, forming a partial thermal well in the HDI layers without affecting the area available for electrical routings. Another option is to form a thermal well by removing the entire HDI layers under the die and attach the die directly to the substrate. This arrangement eliminates the thermal resistance due to the HDI layers but also eliminates the possibility of electrical routings beneath the die. Yet another, compromising option is to place a thermal via network beneath the die on spaced array patterns named via islands, as shown in Fig. 3. The figure also shows the position of a via island array with respect to the die and die attach pad locations. The channels formed between islands make up the typical zone available for routing interconnections. Each of the 4 polyamide dielectric layers between the die attach pad and the ground plane contains an array of vias inter-connecting two adjacent conductive layers to enhance the heat dissipation from the die to a heat sink located below the substrate. The vias are made of copper, and various shapes and different sizes of vias can be embedded within the layers.

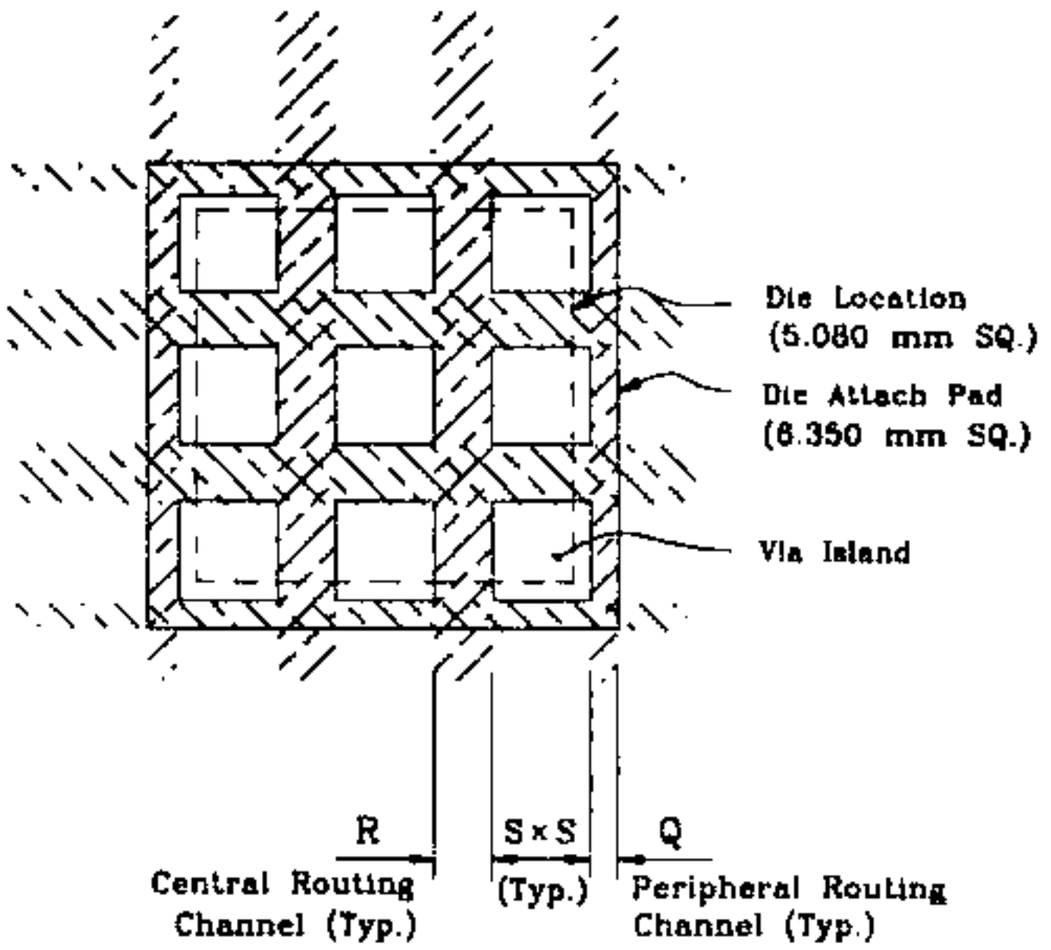

Figure 3: Via Islands and Routing Channels

The resulting arrangement, consisting of the die attach pad, sets of via layers and copper layers embedded under the die, is called the via network. The copper layers within the via network is called the via pads. The typical via layout within a via layer is shown in Fig. 4, and a superposition of all the vias in a 4-layer via network is shown in Fig. 5. The vias are staggered from one layer to the next and there are no vertical overlaps of vias through the layers.

As the size of via islands in a via network increases, the heat removed from a die to a heat sink increases whereas the available electrical routing spaces decreases. An optimal combination between routing density available for the electrical signal lines and

a sufficient area of via network for adequate heat dissipation depends on the type and performance of the chip and the amount of heat that has to be removed from the die to maintain the die temperature under the maximum allowable operating temperature. A single island of via network covering the entire area under a die may have a better capability of removing heat but leaves no routing spaces for electrical signal lines. On the other hand, having no via network leaves entire spaces under the die available for the electrical routings but may results in an unacceptably high die temperature. A via network under a die may consist of a number of small via islands, and the available routing density is determined by dividing the routing channel areas by total available area under the die.

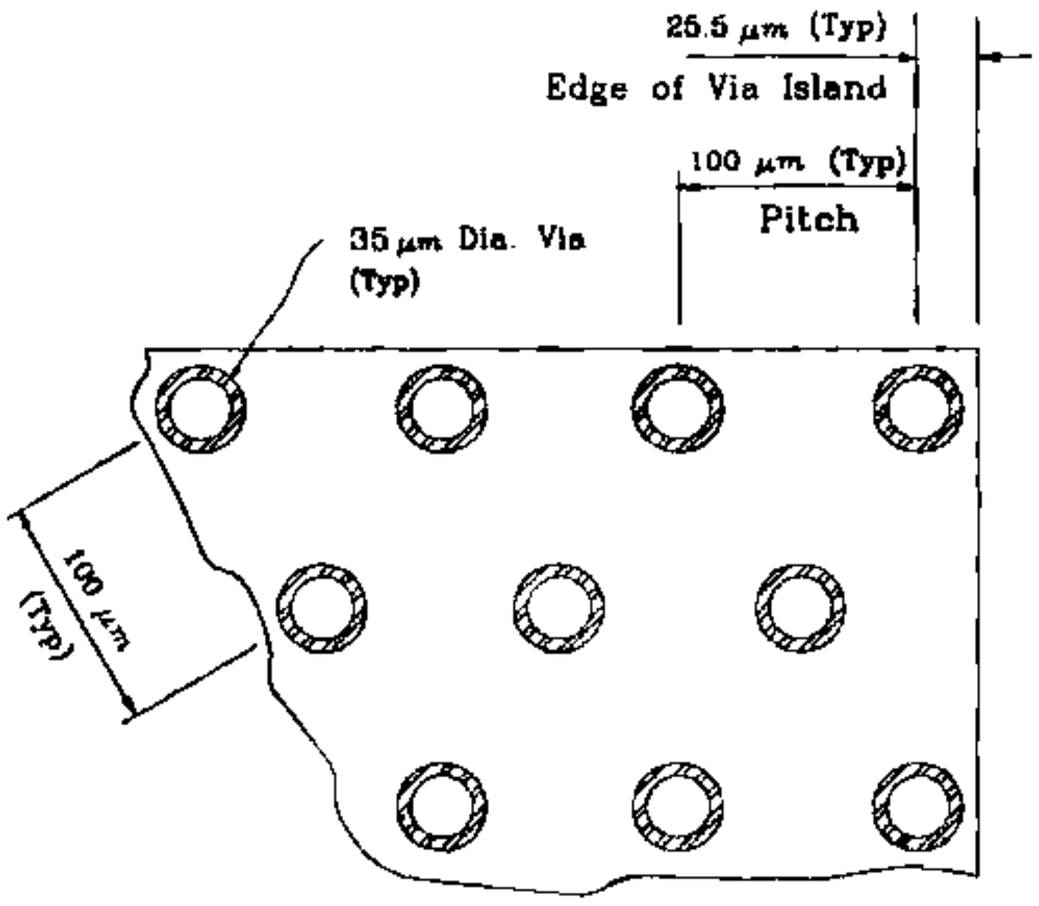

Figure 4: Typical Section View of a Via Layer

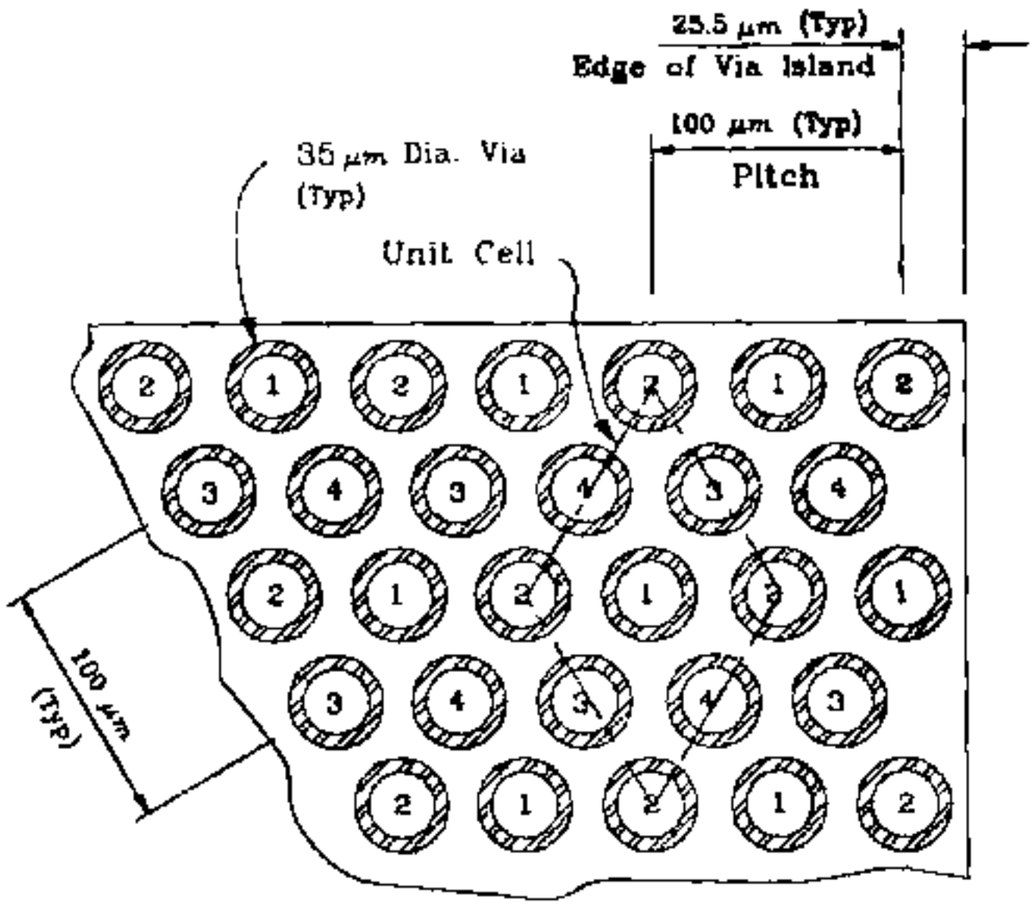

Figure 5: Plan View of a Typical 4-Layer Via Network Shown With All Vias: Numbers Appearing in the Center of Vias Indicate the Via Layer in Which the Via is Located

In order for electrical and thermal designers to determine the optimum routing densities in applications, the heat removal capability of an HDI must be known in estimating the total thermal resistance of the system hence in predicting the operating temperature of the die. It is important, therefore, to have a thermal model that can estimate the effective thermal resistances of a via network and an HDI assembly.

Owing to their high thermal conductivities, it is assumed in the present study that the top surface of the gold die attach pad (k = 310 W/mK) and the bottom surface of the ground plane (k = 386 W/mK) are isothermal. Since this assumption pertains only to the estimation of the effective thermal resistance and, therefore, the effective thermal conductivity of a via network within a system, the differences introduced in the final prediction of the total system resistance and the die operating temperature due to this assumption is not significant. Since the thermal conductivity of polyamide (k = 0.19 W/mK [4]) is 3 orders of magnitude smaller than that of copper, the conduction heat transfer through polyamide within the via network is ignored. However, the analysis accounts for heat dissipation through polyamide channels between via islands by allowing heat to dissipate in parallel paths with heat flow through via islands.

The unit structure of a via network is identified which contains 4 vias in all in its diamond shaped cell, as shown in Fig. 5. Except for the edges of via islands, the entire via structure can be constructed by repeating the unit structure in all four directions. By following the heat paths, it is also identified that there are only three basic geometries that need to be considered in estimating the effective thermal resistance associated with the via network.

For example, the unit structure associated with conduction heat transfer through the die attach pad into a via, or from a via into the 4th via pad can be seen as a hexagonal cell centered at the via, as shown in Fig. 6. This is modeled approximately as a circular disk with an iso-flux heat sink/source over the ring area where the via was attached. This is an axi-symmetric, radial fin problem with one surface being heated/cooled by an isothermal heat source/sink. The distances from the heat source to the outer edges of the original hexagonal structure are large as compared to the source size, and the resulting thermal resistance of the problem would be insensitive to the actual shape of the outer edges. The outer radius of the disk is determined as such the surface area is maintained identical to the original problem. Due to the symmetry of the problem, the outer edge surface of the disk is adiabatic.

Vias are modeled as a tube having inner and outer radii a and b, respectively, and length t. The thermal resistance of vias is computed based on a simple one-dimensional heat conduction analysis.

In analyzing for the intermediate via pads, it can be seen that heat entering into the via pad from a via is conducted through the pad and leaves the pad into four adjacent vias in the next via layer. Each via receives heat that was shared by four vias in the preceding via layer and carries heat that is to be transmitted by four vias in the succeeding via layer. As can be seen from Fig. 7, the unit structure for the via pads is a rectangular area centered at the via. By applying the similar analogy as before, the thermal resistance of this unit can be approximately determined by computing the resistance of a circular disk shown

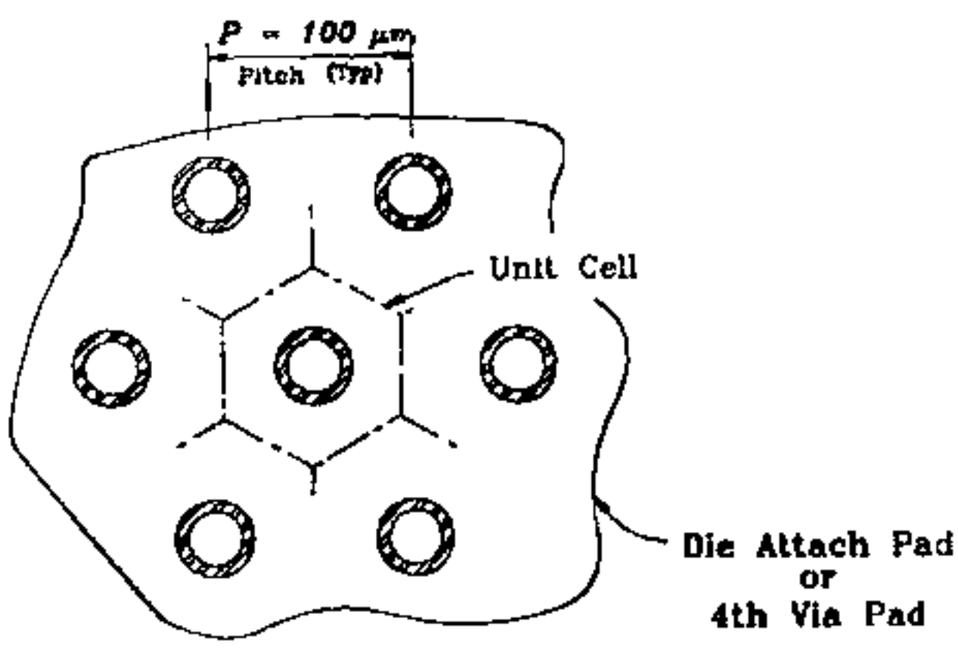

Figure 6: Thermal Modeling of Die Attach Pad or 4th Via Pad

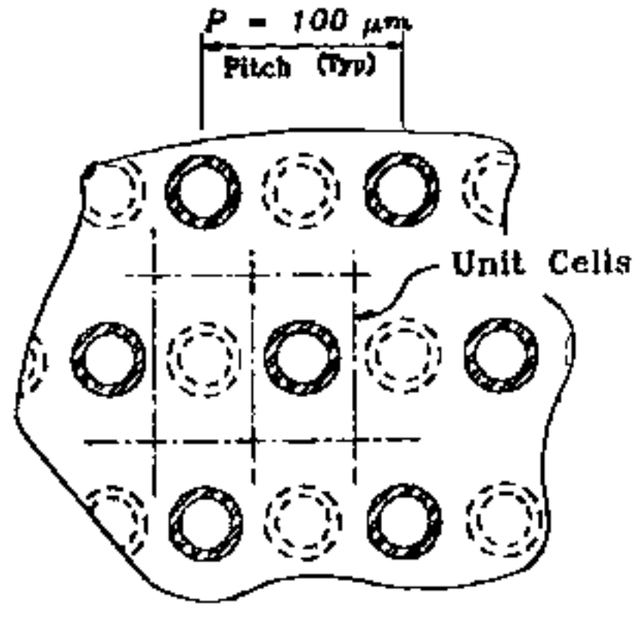

Figure 7: Thermal Modeling of Intermediate Via Pads

in the figure. The disk has a uniform flux ring source/sink on one surface at the center and the iso-thermal edge surface. The remaining surfaces are assumed adiabatic. Again, the outer radius is defined such that the area of the disk is identical to the area of the rectangular unit cell.

The above problems are analytically solved and the thermal resistances of each case can be computed from the following closed form expressions:

$$R_a = \frac{1}{k\pi c_1}\left[t^* + \frac{4}{\alpha^2}\sum_{n=1}^{\infty}\frac{\tanh(\delta_n t^*)}{\delta_n^3}\frac{[b^* J_1(\delta_n b^*) - a^* J_1(\delta_n a^*)]^2}{J_0^2(\delta_n)}\right] \quad (1)$$

$$R_v = \frac{t^*}{k\pi c\alpha} \quad (2)$$

$$R_b = \frac{4}{k\pi c_2 \alpha^2}\sum_{n=1}^{\infty}\frac{1}{\lambda_n^3\tanh(\lambda_n t^*)}\frac{[b^* J_1(\lambda_n b^*) - a^* J_1(\lambda_n a^*)]^2}{J_1^2(\lambda_n)} \quad (3)$$

where

$$\alpha = b^{*2} - a^{*2} \quad (4)$$

R_a and R_b account for the thermal resistances of the die attach pad and the via pads as described in Figs. 6 and 7, respectively, and R_v represents the one-dimensional thermal resistance of a through via. The parameters with the superscript * in Equations (1-3) denote dimensionless quantities that are non-dimensionalized by using length scales c_1, c and c_2, respectively. Note that c in Equation (2) is an arbitrary length scale. J_0 and J_1 are the Bessel functions of the first kind of order 0 and 1, respectively, and δ_n, λ_n are the roots of the Bessel functions:

$$J_1(\delta_n) = 0 \quad (5)$$

$$J_0(\lambda_n) = 0 \quad (6)$$

which satisfy the respective boundary conditions.

By combining the above thermal resistances in a combination of series and parallel paths, the overall thermal resistance of a via island containing N number of vias in total from the top of the die attach pad to the bottom of the ground plane with a 4-layer vias can be obtained as:

$$R_I = \frac{4}{N}(R_{a_D} + 6R_b + 4R_v + R_{a_G}) \quad (7)$$

where R_{a_D} and R_{a_G} are the thermal resistances of the die attach pad and the ground plane (see Fig. 2), respectively. This can then be combined with the thermal resistance of dielectric routing channels in parallel paths. The effective thermal conductivity of a via network can be determined based on the combined thermal resistance.

Package Modeling

From Figs. 1 and 2, it can be seen that the thermal resistance of the via network forms an integral part of the overall package analysis to predict junction temperature rise. The substrate and remaining package characteristics, however, need also be considered in order to adequately address the thermal performance evaluation of the package. Also, the modeling of multichip packages (MCPs) requires the arbitrary specification of die locations.

The complete thermal resistance between the die and substrate can be determined by using the effective thermal conductivity of the via network in a series path with the other layers, allowing for the thermal spreading effect through the via network, the epoxy, the planarizing layer and the layer of thermal grease.

Inclusion of a die resistance into an overall package modeller was recently addressed in [6]. By effectively modeling the die resistance separately, inherently including spreading resistance within the via network, tremendous savings in computational effort can be gained when combined with an overall package modeller. A typical microelectronic package configuration is shown in Figure 8, showing how multiple die heat sources may be found in a standard MCP. As shown, the chips are modelled as heat sources, and the heat leaving the chip surface may follow two possible flow paths as depicted by Fig. 8 (inset). A microelectronic package thermal analyzer as outlined in [6], and incorporated within a PCB analyzer [7], needs to have the capability of including a die interference resistance at the heat source locations. The theoretical procedure for this will now be briefly described. A die contact conductance can be defined in terms of R_{die}, by

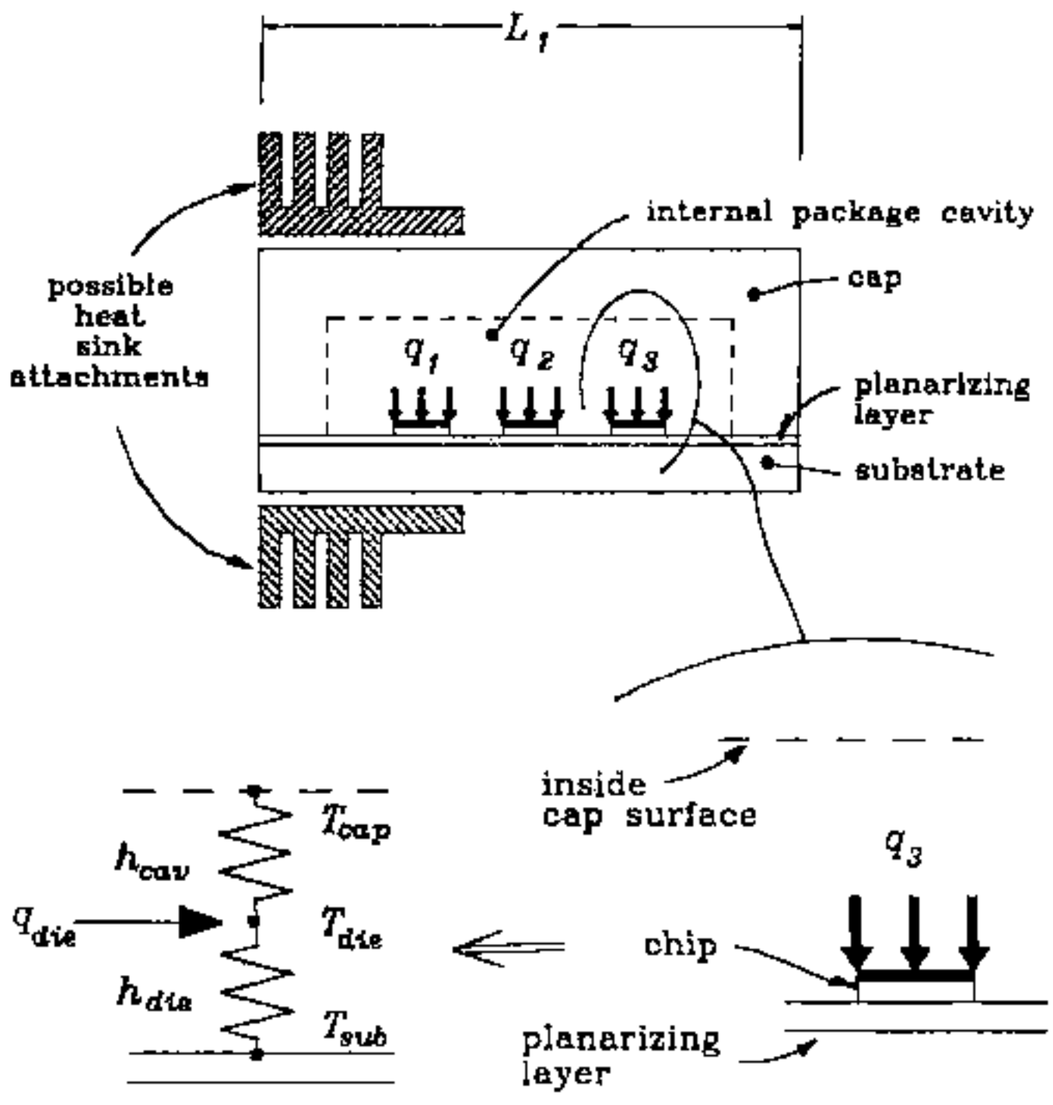

Figure 8: Package Thermal Modeling

$$h_{die} = \frac{1}{A_{die}\, R_{die}} \tag{8}$$

and with this, a heat flux balance at a die-substrate interface can be written into the compact computational form:

$$\frac{L_1 \partial T_s}{\partial z} + Bi\, f_{die}\, (T_s - T_{cap}) = \frac{q_j\, L_1\, f_{die}}{k_s} \tag{9}$$

where f_{die} is defined as

$$f_{die} = (1 + h_{cav}/h_{die})^{-1} \tag{10}$$

and Bi denotes the cavity Biot number:

$$Bi = \frac{h_{cav}\, L_1}{k_s} \tag{11}$$

The length L_1 is a package length as indicated by Fig. 8.

We see that this readily satisfies limiting cases of die resistance. If there was no die resistance between the die and substrate, then

$$R_{die} \to 0,\ h_{die} \to \infty,\ f_{die} \to 1. \tag{12}$$

If the die resistance becomes large, then we must obtain

$$R_{die} \to \infty, h_{die} \to 0, f_{die} \to 0 \tag{13}$$

and thus from Eqn. (9) we would find

$$\frac{\partial T_s}{\partial z} = 0 \tag{14}$$

at the die interface.

This latter condition implies that heat would then flow entirely away from the die into the cavity (ceramic example) and into the package cap layer surface.

The boundary condition specified by Eqn. (9) satisfies the die interface resistance condition, provides for heat loss through Bi to a cavity cap surface, and admits the specified die heat flux. Further details are noted in [6], and we suffice to say that with Eqn. (9), a package modeller can adequately address the inclusion of die interface resistance.

Results and Comparisons

The particular MCP which this study will concern was the same MCP that was recently studied in [3,4]. Since only a single chip was powered up for any given experimental run, the analysis made was essentially as for an SCP, using a total substrate surface area three times the chip ($0.2'' \times 0.2''$) surface area. The experimental MCP did not have a package cap and cavity arrangement as shown by Fig. 8; the die plane surface was exposed to still air ambient conditions.

The results consist of two parts, namely the reporting of vias thermal resistance, and the total thermal resistance of the chip on the MCP system. The latter is the only one which has been

experimentally measured [3,4], the former having been obtained using numerical procedures. Specific details pertaining to the via network are given in Tables 1 and 2.

Via Networks

The models developed for the via network analysis are verified by comparison with numerically reported estimates of the vias thermal resistance [3] in Fig. 9. Since these are purely numerical predictions obtained by using a finite element method, the results shown reflect a thermal conductivity of polyamide, $k_{poly} = 0.46\ W/mK$, which was used in [3], rather than the value (0.19) shown in Table 1. It is important to note that the values shown in Fig. 9 are *specific* thermal resistances ($\equiv R_{die} \times A_{die}$) of the via network. This means that the plotted results are applicable to various die sizes; values obtained from the plot need to be divided by a die surface area to obtain the actual thermal resistance.

Table 1: Dimensions and Thermal Conductivities [3,4]

Item	Dimensions (μm)	k (W/mK)
Die	5080 × 5080 × 25	150
Thermal Epoxy	5 (thickness)	3.8
Die Attach Pad	6350 × 6350 × 5	310
Planarizing Layer	5 (thickness)	0.19
HDI Dielectric, Polyamide Layers	5 (thickness)	0.19
HDI Conductive Layers, Via Pads	5 (thickness)	386
Vias	35 O.D. × 28 I.D. × 5	386
Ceramic substrate	1016 (thickness)	30
Grease Layer	25 (thickness)	0.8

Table 2: Routing Availability and Dimensions of Via Islands

Routing (%)	S (mm)	R (mm)	Q (mm)	No. of Vias per Island	No. of Islands
0	5.900	—	0.225	3973	1
20	1.683	0.520	0.120	314	9
40	1.233	1.063	0.260	168	9
75	0.508	1.950	0.470	25	9
100	—	—	—	—	—

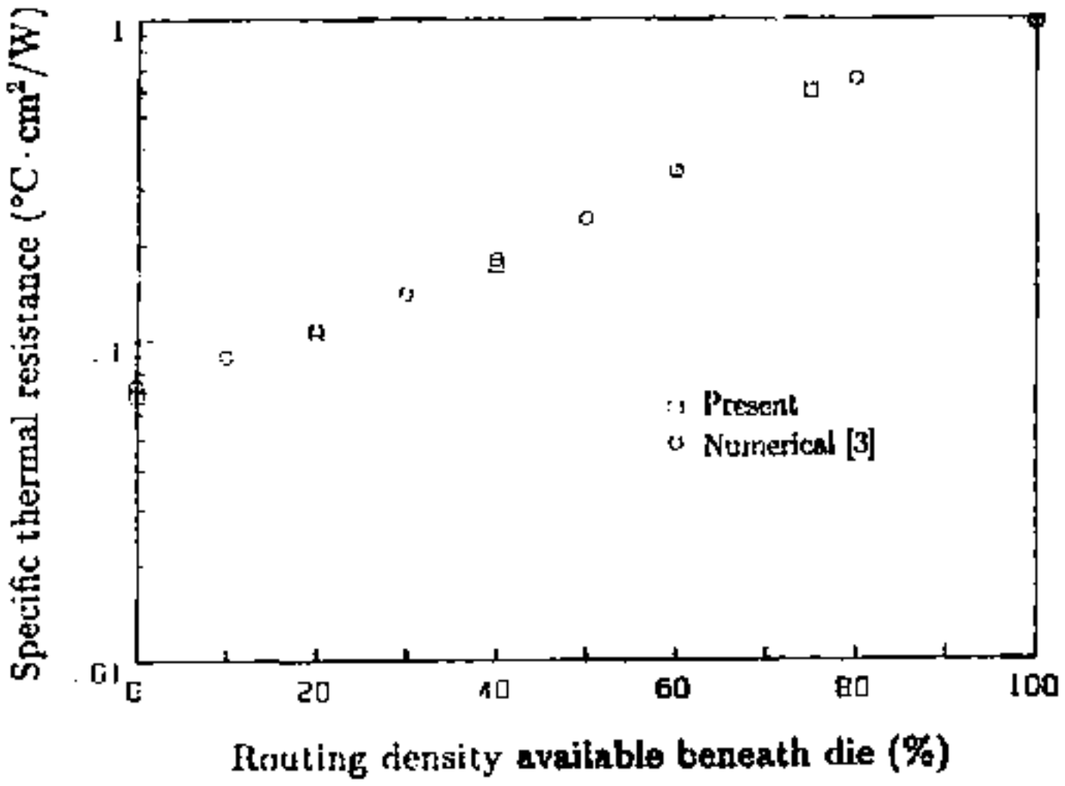

Figure 9: Comparison of Specific Thermal Resistances For Via Networks with No Planarizing Layer

The agreement between reported estimates [3] and the predictions obtained from this study is very good. The unit via cell analysis outlined earlier, and summarized by Eqns. (1–6), thereby provides a highly accurate and quick estimate of the complex via network. The solutions were determined quite easily and quickly (< 20 sec) using an IBM PC-AT.

Package Modeling

Thermal resistance measurements were obtained [3,4] from various chips mounted on an MCP. Using $0.2'' \times 0.2''$ chips, thermal resistances ($R_{tot} \equiv (T_j - T_{amb})/Q_j$) are shown in Fig. 10 for various routing densities and thermal enhancement options. The system was analyzed using an efficient package modeller [6] which allowed for inclusion of a die and vias thermal resistances as discussed earlier. The agreement was found to be good except for the 40% and 75% routing cases. The analytical predictions for these cases however, are consistent with the changes in vias thermal resistance. From 20% to 40% routing density, the computed via network resistance changed from $R_{vias} = 0.196\ °C/W$ to $R_{vias} = 0.342\ °C/W$, yet the measured change in total system thermal resistance went from $R_{tot} = 2.72\ °C/W$ to $R_{tot} = 3.6\ °C/W$. It is anticipated that this slight discrepancy may be adjusted upon further examination of experimental setup and data.

Conclusions

A detailed description of an analytically developed, thermal vias model has been presented. The model makes use of closed-form expressions for thermal resistances which may be easily implemented into any particular chip-attachment thermal resistance analysis of a microelectronic package.

Results show very good agreement with recently reported numerical and experimental data for a complete range of routing density. Further general studies are recommended to pursue the effectiveness of die attachment and planarizing layers, as well as the procurement of proper effective thermal conductivities.

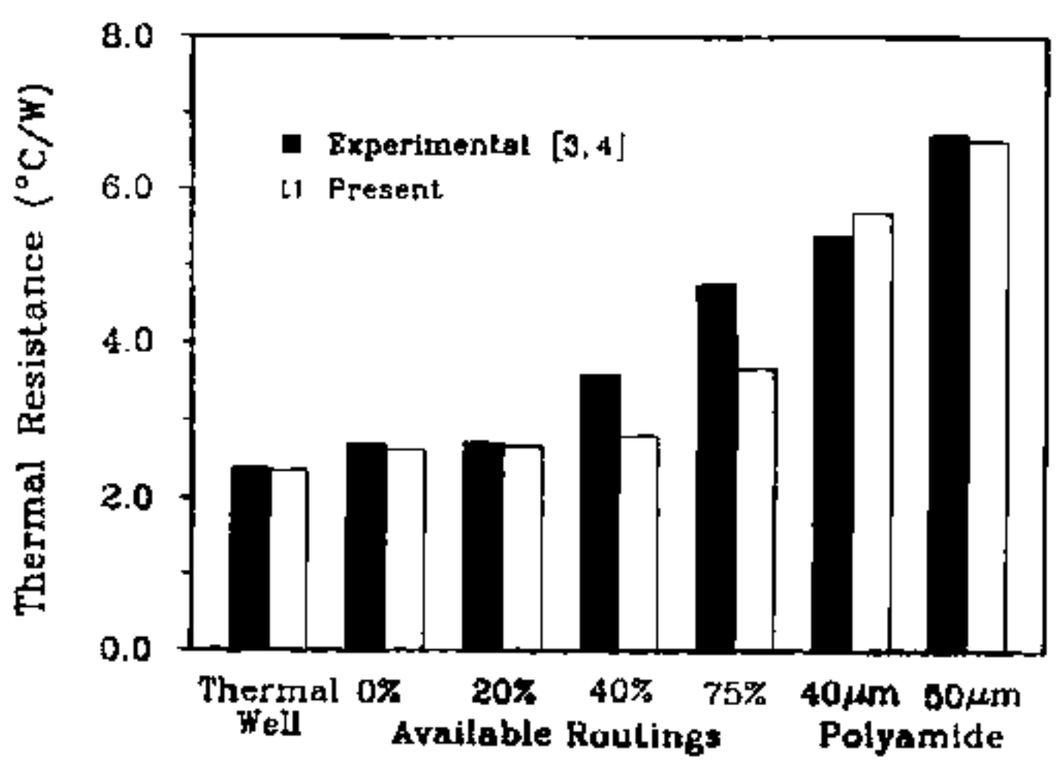

Figure 10: Comparison of Package Thermal Resistances With Various Thermal Enhancement Options

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