AN INTRODUCTION TO THERMAL-ELECTRICAL COUPLING IN BIPOLAR TRANSISTORS

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ABSTRACT

An approximate model to illustrate thermal-electrical coupling in bipolar transistors has been developed with a thermal model that accounts for two-dimensional, non-linear heat conduction in a particular transistor structure. The effect of thermal-electrical coupling on the terminal characteristics of the device is shown to be substantial and the phenomenon of thermal instability or thermal runaway is also demonstrated using this thermal-electrical model. A parametric study of a hypothetical transistor shows that major improvements in the operating range of a bipolar transistor can be realized through decreased thermal resistance.

NOMENCLATURE

a - half-width of emitter stripe
A - total emitter area
b - half center-to-center spacing of adjacent emitter stripes
D_n - diffusion constant for electrons
e - electronic charge
E_g - bandgap
g_m - transconductance
G_b - base Gummel number
$H(\cdot)$ - Heaviside Unit Step Function
I_B - base current
I_C - collector current
$I_{C\,max}$ - maximum allowable collector current for a given V_{CE}
I_{Cu} - collector current at onset of thermal instability
I_{max} - maximum allowable collector current for any V_{CE}
k - thermal conductivity
L_{eff} - effective emitter length
n_i - intrinsic carrier concentration
N^* - constant used in modelling n_i
p - power law coefficient for thermal conductivity model
q - heat flux
Q - total power dissipation
R_t - linearized thermal resistance of the transistor

R_∞ - thermal resistance exterior to the silicon die
R_{EE} - finite emitter electrical resistance
t - thickness of die
T - temperature
T_b - temperature at base of die
$\bar{T}_c$ - average or representative emitter contact temperature
T_∞ - ambient temperature
U - transformed temperature
V_{BE} - forward bias of base to emitter
V_{CE} - reverse bias of collector to emitter
V_{br} - breakdown voltage of transistor
x, z - Cartesian coordinate system

Greek Symbols

α - aspect ratio of unit cell ($\equiv t/b$)
ϵ - relative emitter width ($\equiv a/b$)
λ - Boltzmann's constant
μ_n - electron mobility

Subscripts

B - refers to base of transistor
C - refers to collector of transistor
E - refers to emitter of transistor
n - refers to series solution
∞ - refers to ambient conditions

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INTRODUCTION

In recent years the cooling of integrated circuit chips in electronic equipment has received considerable attention. The reasons usually cited for this concern about excessively high temperatures in semiconductor devices are ones of degradation of reliability due to both performance variations and component failures. These concerns are quite legitimate. For example, with field-effect devices high temperature operation results in large threshold voltage changes, lower channel mobility (or slower "speed"), and an exponential increase in leakage currents. In logic applications any one or all of these effects can lead to substantial increases in error rates. Furthermore, with bipolar devices there exists a problem where thermal instability can lead potentially to physical destruction of the transistor. Yet another

concern is that of fatigue failures of metal interconnects due to high temperature cycling. However, even in the absence of these "excessive" or "damaging" temperatures, an incentive to compute device temperatures still exists simply to accurately predict the electrical performance of semiconductor devices in real circuits. This is especially true for bipolar transistors where in many cases the coupling between the thermal and electrical device performance can be quite strong. The goal of this work is to demonstrate how parameters which appear to affect only the thermal characterization of a bipolar transistor can also influence considerably the electrical performance of the device. This goal is achieved by developing a realistic approximate model for heat conduction in a high-power transistor structure and then coupling this model with an extremely simplified electrical model for the bipolar transistor.

THEORETICAL DERIVATION

Thermal Model

An idealized view of a large-scale bipolar transistor which might be used for high-power switching applications is shown in Fig. 1. This transistor consists of multiple emitter "fingers" which act electrically in parallel. For many typical transistors where the thickness of the silicon die is on the order of 200 μm, most of the voltage drop in the device occurs directly underneath the emitter contacts within several μm from the surface. Thus the non-uniform heat generation within the device is often approximated by a uniform heat flux applied to the emitter contact as in the previous work of Latif (1979) and Katsueda, et al. (1984). The actual magnitude of this heat flux, however, will be shown in the next section to be a complex function of the transistor biasing conditions and the emitter contact temperature. The geometric symmetry of the transistor structure shown in Fig. 1 can also be utilized to simplify the model for heat conduction in the silicon die. By further assuming that the heat conduction is predominantly two-dimensional since the emitter stripe lengths are often much larger than the die thickness, an approximate model which characterizes heat conduction in the transistor is derived as shown in Fig. 2.

Heat conduction in the silicon die as modeled in Fig. 2 is governed by the partial differential equation

$$\nabla \cdot (k(T)\nabla T) = 0 \qquad (1)$$

subject to the boundary conditions

$$k(T(x,0))\frac{\partial T}{\partial z}(x,0) = qH(a-x) \qquad 0 \le x \le b \qquad (2)$$
$$T(x,t) = T_b \qquad 0 \le x \le b \qquad (3)$$
$$\frac{\partial T}{\partial x}(0,z) = 0 \qquad 0 \le z \le t \qquad (4)$$
$$\frac{\partial T}{\partial x}(b,z) = 0 \qquad 0 \le z \le t \qquad (5)$$

where $H(\cdot)$ is the Heaviside Unit Step Function and T_b the temperature at the base of the die.

Note that the temperature-dependent thermal conductivity of the silicon die creates a non-linear problem. Fortunately, Ozisik (1980) has shown that an entirely linear problem can be used to characterize Eqs. (1) to (5) by introducing the integral transformation

$$U = \int_{T_{ref}}^{T} \frac{k(T')}{k(T_{ref})} dT' \qquad (6)$$

For both silicon and gallium arsenide, excellent correlations of available data for thermal conductivity versus temperature (Maycock, 1967) can be made using the form
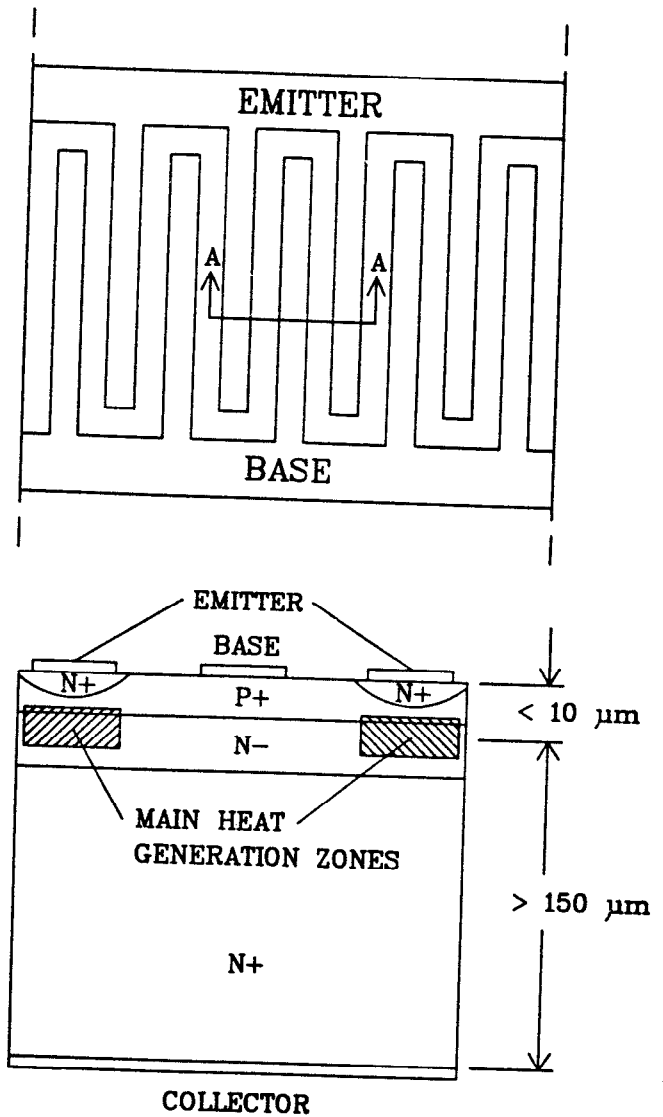

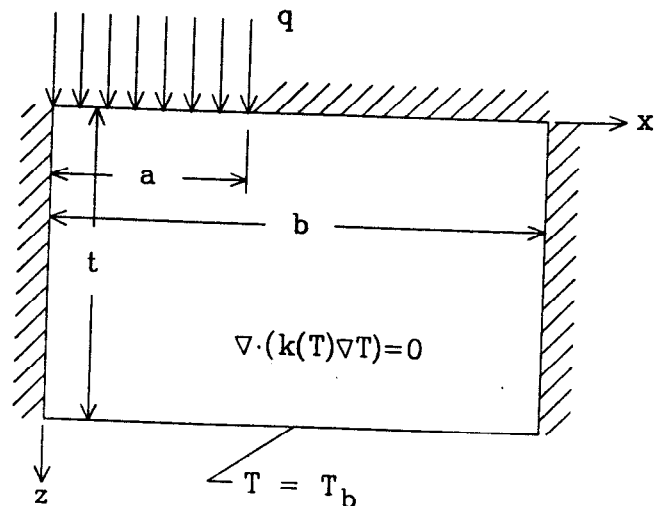Fig. 1 Typical bipolar transistor structure for high-power switching applications

Fig. 2 Idealized thermal model for transistor

$$k(T) = k_\infty \left(\frac{T}{T_\infty} \right)^p \qquad (7)$$

where k_∞ is the thermal conductivity at the ambient temperature T_∞ (usually 300 K) and p is determined to best fit the experimental data. With $k(T)$ given by Eq. (7) and T_{ref} set to T_∞, transformed temperature in the silicon die is then

$$U = \frac{T_\infty}{p+1} \left[\left(\frac{T}{T_\infty} \right)^{p+1} - 1 \right] \qquad (p \neq -1) \qquad (8)$$

or conversely

$$T = T_\infty \left[1 + (p+1)\frac{U}{T_\infty} \right]^{\frac{1}{p+1}} \qquad (9)$$

In terms of the transformed temperature Eqs. (1) to (5) become

$$\nabla^2 U = 0 \qquad (10)$$

$$k_\infty \frac{\partial U}{\partial z}(x,0) = qH(a-x) \qquad 0 \leq x \leq b \quad (11)$$

$$U(x,t) = \frac{T_\infty}{p+1} \left[\left(\frac{T_b}{T_\infty} \right)^{p+1} - 1 \right] \qquad 0 \leq x \leq b \quad (12)$$

$$\frac{\partial U}{\partial x}(0,z) = 0 \qquad 0 \leq z \leq t \quad (13)$$

$$\frac{\partial U}{\partial x}(b,z) = 0 \qquad 0 \leq z \leq t \quad (14)$$

A solution to this linear problem can be derived analytically using the method of separation of variables. Consideration of Eqs. (10), (13) and (14) leads to the series solution (Negus and Yovanovich, 1986)

$$U = C + Dz + \sum_{n=1}^{\infty} \left[A_n \cosh \frac{n\pi z}{b} + B_n \sinh \frac{n\pi z}{b} \right] \cos \frac{n\pi x}{b} \qquad (15)$$

Application of the boundary condition at the base of the die (Eq. (12)) yields

$$D = -\frac{q\epsilon}{k_\infty} \qquad (16)$$

$$C = \frac{qa}{k_\infty}\alpha + \frac{T_\infty}{p+1} \left[\left(\frac{T_b}{T_\infty} \right)^{p+1} - 1 \right] \qquad (17)$$

$$B_n = -A_n \coth n\pi\alpha \qquad (18)$$

The aspect ratio α and the relative emitter width ϵ are defined as

$$\alpha \equiv t/b \qquad (19)$$

$$\epsilon \equiv a/b \qquad (20)$$

where t is the thickness of the silicon die, a the half-width of the emitter stripe, and b half the center-to-center spacing of adjacent emitter stripes.

The remaining unknowns, the A_n, are determined by applying the orthogonality property of the eigenfunctions $\cos(n\pi x/b)$ to Eq.(11) to give

$$A_n = \frac{2qb \sin n\pi\epsilon}{k_\infty n^2 \pi^2 \coth n\pi\alpha} \qquad (21)$$

A thermal resistance for the transistor is now defined as

$$R_t = \frac{\bar{U}_c - U(z=t)}{Q} \qquad (22)$$

where the average transformed contact temperature is

$$\bar{U}_c = \frac{1}{a} \int_0^a U(x,0)dx \qquad (23)$$

and the total power dissipation of the transistor is related to the uniform heat flux q according to

$$Q = 2L_{eff}aq \qquad (24)$$

where L_{eff} is the effective total emitter stripe length. An analytical expression for R_t can then be derived as

$$R_t = \frac{1}{2k_\infty L_{eff}} \left\{ \alpha + \frac{2}{\pi^3 \epsilon^2} \sum_{n=1}^{\infty} \frac{\sin^2 n\pi\epsilon}{n^3} \tanh n\pi\alpha \right\} \qquad (25)$$

From Eq. (9) an average or "representative" emitter contact temperature is

$$\begin{aligned}\bar{T}_c &= T_\infty \left[1 + (p+1)\frac{\bar{U}_c}{T_\infty} \right]^{\frac{1}{p+1}} \\ &= T_\infty \left[\frac{p+1}{T_\infty}QR_t + \left(\frac{T_b}{T_\infty} \right)^{p+1} \right]^{\frac{1}{p+1}}\end{aligned} \qquad (26)$$

The base temperature at the bottom of the silicon die is related to the ambient temperature by the simple relationship

$$T_b = T_\infty + QR_\infty \qquad (27)$$

where R_∞ is the external thermal resistance from the die to ambient. The average emitter temperature of the bipolar transistor described in this work is then expressed in terms of the power dissipation Q and the resistances R_t and R_∞ according to

$$\bar{T}_c = T_\infty \left[\frac{p+1}{T_\infty}QR_t + \left(1 + \frac{QR_\infty}{T_\infty} \right)^{p+1} \right]^{\frac{1}{p+1}} \qquad (28)$$

Electrical Model

In the previous section a relationship between the average emitter temperature and the power dissipation of the transistor has been derived. In this section a simplified electrical model of the transistor is presented to provide a second relationship between power dissipation and average emitter temperature. A schematic diagram of a bipolar transistors as a three-terminal device is shown for the common-emitter configuration in Fig. 3. In most applications where the
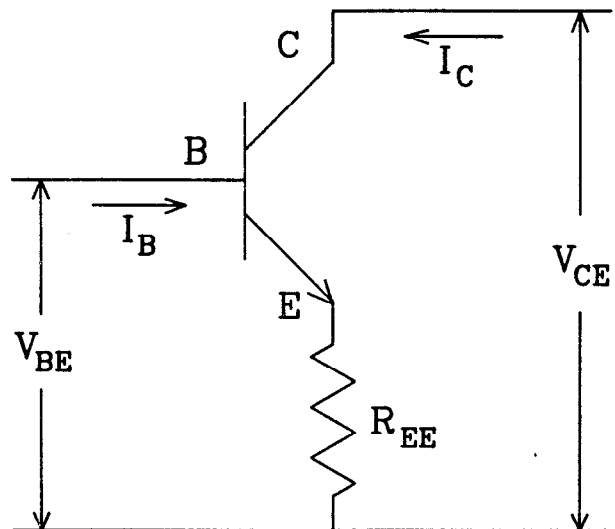

Fig. 3 Schematic representation of transistor for common-emitter configuration

bipolar transistor is useful, the collector current I_C is much greater than the base current I_B and the collector-emitter bias V_{CE} is much greater than the base-emitter bias V_{BE}. For this case of $I_C \gg I_B$ and $V_{CE} \gg V_{BE}$ the power dissipation of the transistor is approximately

$$Q = I_C V_{CE} \qquad (29)$$

The goal of a bipolar transistor model is usually to accurately relate I_C to V_{CE} and V_{BE}. One model which provides realistic predictions for many transistors is the Gummel-Poon model as described by Getreu (1978). With some further assumptions this model can be simplified to

$$I_C = \frac{eAn_i^2 D_n}{G_b} \exp\left[\frac{e}{\lambda T}(V_{BE} - I_C R_{EE})\right] \qquad (30)$$

for the transistor illustrated schematically in Fig. 3. In this model e is the electronic charge ($e = 1.60 \times 10^{-19}$ Coulombs) and λ is Boltzmann's constant ($\lambda = 8.62 \times 10^{-5}$ eV/K). The effective emitter area is A and the base Gummel number is G_b. In this work G_b is treated as a process constant for a given transistor although in reality it is a non-linear function of V_{BE} and V_{CE}. This model also assumes that the transistor is maintained at some uniform temperature T which is obviously not entirely justified. However, the region which most affects the collector current I_C is the emitter-base junction. Since the emitter-base junction is typically within a few μm from the top surface of the die, this region can be approximated as uniform in temperature with a value given by the average emitter temperature $\bar{T}_c$ (often referred to as the "junction" temperature). The diffusion constant for electrons D_n is related to the electron mobility μ_n for moderate base doping levels by the Einstein relationship (Sze, 1981).

$$D_n = \frac{\lambda T}{e}\mu_n \qquad (31)$$

where the mobility versus temperature relationship can often be modeled as (Sze, 1981)

$$\mu_n = \mu_{n\infty}\left(\frac{T}{T_\infty}\right)^{-3/2} \qquad (32)$$

The intrinsic carrier concentration n_i can be shown to be (Sze, 1981)

$$n_i^2 = N^* T^3 \exp\left[-\frac{E_g}{\lambda T}\right] \qquad (33)$$

where for silicon $N^* \approx 1.08 \times 10^{31} \mathrm{cm}^{-6}\mathrm{K}^{-3}$ and $Eg \approx 1.1$ eV for $300 < T < 500$ K.

Upon replacing T by $\bar{T}_c$ and substituting Eqs. (31) – (33) into Eq. (30), the electrical model for I_C becomes

$$I_C = \frac{\lambda \mu_{n\infty} A N^* T_\infty^{3/2}}{G_b}\bar{T}_c^{5/2} \exp\left[\frac{e(V_{BE} - I_C R_{EE}) - E_g}{\lambda \bar{T}_c}\right] \qquad (34)$$

If I_C and V_{CE} are specified for a given transistor, the average emitter temperature can be computed directly from Eqs. (28) and (29). Inversion of Eq. (34) then gives the base-emitter bias as

$$V_{BE} = I_C R_{EE} + \frac{E_g}{e} + \frac{\lambda \bar{T}_c}{e}\ln\left[\frac{I_C G_b}{\lambda \mu_{n\infty} A N^* T_\infty^{3/2}\bar{T}_c^{5/2}}\right] \qquad (35)$$

TERMINAL CHARACTERISTICS

The importance of thermal analysis to the accurate prediction of bipolar transistor performance can be illustrated by examining the terminal characteristics of a device both with and without consideration of thermal-electrical coupling. The bipolar transistor to be

studied has all of its parameters pertinent to the preceding analysis listed in Table 1. This transistor, although hypothetical, is loosely based on a device studied by Latif (1979) and is indicative of a high-power switching device attached to a copper heat sink. Note that the device also has a maximum collector current limit, I_{max}, and a maximum collector-emitter voltage, V_{br}. These limits arise from physical phenomena which are not accounted for in the extremely simplified electrical model of this work.

Typical terminal characteristics for this device are illustrated in Fig. 4 for the default parameter values in Table 1. The solid curve of Fig. 4 reflects the I_C versus V_{BE} behaviour for fixed V_{CE} as predicted by the thermal-electrical model derived in this work. The dashed curves are predictions of I_C versus V_{BE} for fixed device temperatures where thermal-electrical coupling is ignored. An inspection of Fig. 4 shows that substantial errors in the prediction of I_C for a given V_{BE} and V_{CE} can result when fixed device temperatures are assumed. Furthermore even larger errors occur in the prediction of the transconductance of the device. Transconductance is an important parameter in predicting small-signal device response and is defined as

Parameter	Default Value
a	20 μm
b	60 μm
t	200 μm
L_{eff}	1 cm
T_∞	300 K
k_∞	1.31 W/cm·K
p	−1.33
R_∞	1 K/W
G_b	10^{13} cm^{-2}
$\mu_{n\infty}$	300 cm^2/V·s
R_{ee}	.14 Ω
I_{max}	12 A
V_{br}	200 V
T_{max}	500 K

Table 1. Default values of physical parameters for the transistor under study
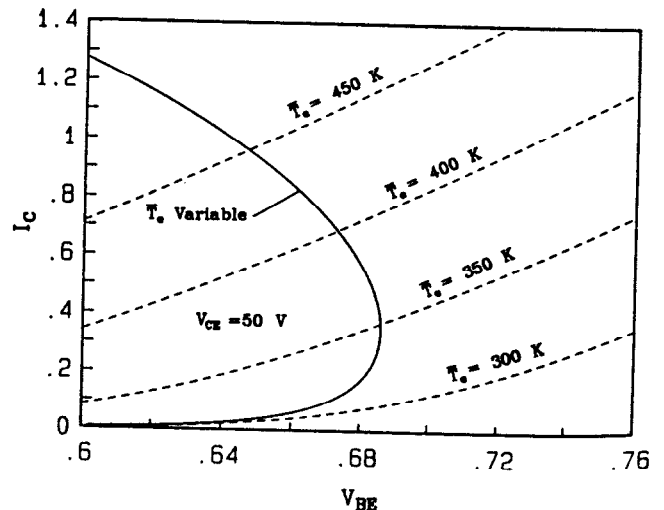

Fig. 4 Terminal characteristics for default transistor at $V_{CE} = 50$ V

$$g_m = \frac{\partial I_C}{\partial V_{BE}}\bigg|_{V_{CE}} \qquad (36)$$

or essentially the slope of the I_C versus V_{BE} curve. With the simple electrical model assumed in this work, g_m is always found to be positive and finite when thermal-electrical coupling is ignored. However, Fig. 4 shows that in reality the transconductance can become unbounded and even negative with increasing collector current I_C for fixed V_{CE}.

THERMAL INSTABILITY AND SAFE OPERATING AREA

For most practical purposes bipolar transistors can not be operated in the negative-transconductance (or negative-differential resistance) region of Fig. 4. A major reason for this is the potentially destructive instability which can result when attempting to turn off the device. For example, consider the transistor described in Table 1 operating as shown in Fig. 4 at $V_{BE} = .664\ V$, $I_C = .8\ A$, $\bar{T}_c = 420$ K, and $V_{CE} = 50$ V. If one attempts to turn off the device by decreasing V_{BE} over a sufficient period of time then I_C will actually increase. As the collector current increases the emitter temperature also increases as indicated on Fig. 4 and eventually leads to actual physical destruction of the device if uncontrolled. An example of such a situation occurs with discrete power devices used to switch large inductive loads such as AC motors. In these applications switching occurs over several milliseconds or longer which thus leads to component failures as described in Latif (1979). This phenomenon is often referred to as thermal instability or thermal runaway and has been the catastrophic failure mechanism for countless bipolar transistors in many different applications over the past 30 years.

The actual operating point at which thermal instability can begin to occur is determined by examining the differential resistance of the transistor. As shown in Fig. 4 the transition to a negative-transconductance region occurs when this differential resistance is zero. From Eq. (35) the differential resistance can be derived as

$$\frac{\partial V_{BE}}{\partial I_C}\bigg|_{V_{CE}} = R_{EE} + \frac{\lambda}{e}\left\{\frac{\bar{T}_c}{I_C} + \frac{\partial \bar{T}_c}{\partial I_C}\bigg|_{V_{CE}}\left[\ln\left(\frac{I_C G_b}{\lambda \mu_{n\infty} A N^* T_\infty^{3/2} \bar{T}_c^{5/2}}\right) - \frac{5}{2}\right]\right\} \qquad (37)$$

where Eqs. (28) and (29) can be combined to give

$$T_c = T_\infty\left[\frac{p+1}{T_\infty}R_t V_{CE} I_C + \left(1 + \frac{R_\infty V_{CE} I_C}{T_\infty}\right)^{p+1}\right]^{\frac{1}{p+1}} \qquad (38)$$

and with some algebraic manipulation,

$$\frac{\partial T_c}{\partial I_C}\bigg|_{V_{CE}} = \left(\frac{T_\infty}{\bar{T}_c}\right)^p V_{CE}\left[R_t + R_\infty\left(\frac{R_\infty V_{CE} I_C}{T_\infty}\right)^p\right] \qquad (39)$$

The collector current above which the transistor will be thermally unstable, I_{Cu}, is thus given for a particular V_{CE} by

$$\frac{\partial V_{BE}}{\partial I_C}\bigg|_{V_{CE}}(I_C = I_{Cu}) = 0 \qquad (40)$$

This current represents an upper bound on the allowable collector current for a given V_{CE}. In many cases though the transistor may be thermally limited at collector currents below I_{Cu} due simply to intolerable temperature rises within the die. The maximum temperature limitation may arise from factors such as limits on expansion of metal interconnects on the die or unacceptable variation of device behaviour over wide temperature ranges. Manufacturers usually supply a curve called the Safe Operating Area or SOA of the transistor which shows graphically the maximum allowable collector current for the entire range of V_{CE}. A typical SOA curve is shown in

Fig. 5 for the default transistor described in Table 1. The curve can be described in terms of three distinct regions. In region 1 the device is electrically limited to a maximum current I_{max} for reasons which will not be discussed in this work. Region 2 is essentially bounded by a constant power dissipation curve ($I_{C\,max} V_{CE} = Q_{max}$) corresponding to the maximum allowable temperature for the transistor (assumed to be 500 K in this case). Thermal instability as described by Eqs. (37) – (40) limits the collector current to $I_{C\,max} = I_{Cu}$ in region 3 which is also terminated by a maximum voltage limitation.

The next sections examine how variations in parameters which describe the transistor's physical system affect the device performance and SOA curve. Obviously a decrease in overall thermal resistance will increase the Safe Operating Area in region 2 by allowing a higher maximum power dissipation for a given maximum temperature. It is not obvious beforehand, however, what effect thermal resistance has on the thermal instability which limits the collector currents in region 3 of the SOA curve.

EFFECT OF EMITTER SPACING AND DIE THICKNESS

Variation of the emitter spacing or die thickness of the transistor will obviously affect the internal thermal resistance of the transistor. General trends for the effect of transistor geometry on $I_{C\,max}$ can be investigated using the thermal-electrical model developed in this work. The results are presented in tabular form for $V_{CE} = 10$ V and $V_{CE} = 50$ V.

The effect of varying emitter spacing is presented in Table 2 by using values of b from 50 to 100 μm. For $V_{CE} = 10$ V the current limitation arises from the requirement that $\bar{T}_c$ not exceed 500 K. Increased emitter spacing decreases the internal thermal resistance and thus allows higher collector currents for a given maximum temperature. When $V_{CE} = 50$ V the current limitation is due to thermal instability occurring at temperatures far below $T_{max} = 500$ K. Changes in emitter spacing are seen to have a more pronounced effect on $I_{C\,max}$ in this case. This can be explained by noting that decreased thermal resistance causes thermal instability to occur at higher temperatures as reported in Table 2. Thus $I_{C\,max}$ can be increased considerably in this region by increasing the emitter spacing. The major penalty to be paid for increasing emitter spacing is one of inefficient utilization of available silicon area.

In Table 3 $I_{C\,max}$ is given as a function of the die thickness with all other physical parameters assumed to have their default values. The general trends observed are similar to those of Table 2. When
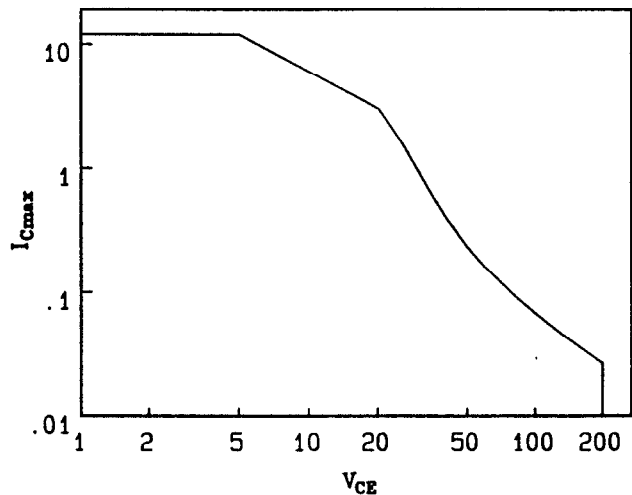

Fig. 5 Safe Operating Area for default transistor

b (μm)	$V_{CE} = 10$ V		$V_{CE} = 50$ V	
	$I_{C\,max}$ (A)	$\bar{T}_c(I_{C\,max})$ (K)	$I_{C\,max}$ (A)	$\bar{T}_c(I_{C\,max})$ (K)
50	5.50	500	.193	327
55	5.74	500	.212	328
60	6.00	500	.231	330
65	6.22	500	.248	331
70	6.42	500	.265	332
75	6.60	500	.282	334
80	6.76	500	.298	335
90	7.05	500	.327	337
100	7.28	500	.355	339

Table 2. Variation of $I_{C\,max}$ and $\bar{T}_c(I_{C\,max})$ versus emitter spacing

R_{∞} (K/W)	$V_{CE} = 10$ V		$V_{CE} = 50$ V	
	$I_{C\,max}$ (A)	$\bar{T}_c(I_{C\,max})$ (K)	$I_{C\,max}$ (A)	$\bar{T}_c(I_{C\,max})$ (K)
.50	7.32	500	.380	340
.75	6.59	500	.288	334
1.00	6.00	500	.231	330
1.25	5.52	500	.190	327
1.50	5.13	500	.162	325
2.00	4.49	500	.124	322
3.00	3.62	500	.084	319
5.00	2.62	500	.050	317

Table 4. Variation of $I_{C\,max}$ and $\bar{T}_c(I_{C\,max})$ versus external thermal resistance

t (μm)	$V_{CE} = 10$ V		$V_{CE} = 50$ V	
	$I_{C\,max}$ (A)	$\bar{T}_c(I_{C\,max})$ (K)	$I_{C\,max}$ (A)	$\bar{T}_c(I_{C\,max})$ (K)
150	7.00	500	.323	337
175	6.46	500	.270	333
200	6.00	500	.231	330
225	5.61	500	.201	328
250	5.26	500	.179	326
300	4.69	500	.145	323
350	4.23	500	.122	322
400	3.86	500	.106	321
500	3.28	500	.082	319

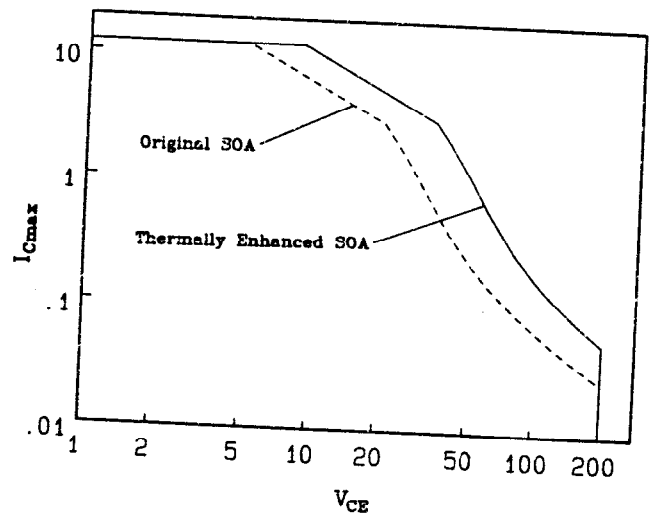Table 3. Variation of $I_{C\,max}$ and $\bar{T}_c(I_{C\,max})$ versus die thickness

Fig. 6 Increased Safe Operating Area for thermally enhanced transistor

the die thickness is increased the thermal resistance increases and $I_{C\,max}$ is reduced. For the thermal instability region ($V_{CE} = 50\ V$) the decrease in $I_{C\,max}$ can be substantial.

EFFECT OF EXTERNAL THERMAL RESISTANCE

In Table 4 $I_{C\,max}$ is reported for different values of the thermal resistance R_{∞} from the base of the die to ambient. As expected $I_{C\,max}$ decreases as R_{∞} increases. This indicates that the performance range for a given transistor can be greatly increased by providing a superior heat dissipation system.

A transistor with increased emitter spacing, decreased die thickness and decreased external thermal resistance should have an increased Safe Operating Area. With the "best" parameter values from Tables 2–4 used to describe a thermally enhanced transistor (b=100 μ m, t=150 μ m, R_{∞} = .5 K/W), the increase in SOA from the default transistor is shown in Fig. 6.

CONCLUSIONS

An approximate model has been developed to describe thermal-electrical coupling in bipolar transistors. The electrical model is extremely simplified but the thermal model consists of an analytical solution for two-dimensional heat conduction with non-linear thermal conductivity. The methodology could also be extended to more complex transistor models and to three-dimensional thermal models.

Thermal-electrical coupling has been found to have a major effect on the terminal characteristics of a bipolar transistor. This coupling also leads to thermal instability which can limit the tolerable current through the device. In some cases thermal instability can occur at device temperature rises of less than 20°C above ambient.

A parametric study for a hypothetical transistor has revealed that decreasing the thermal resistance of the system permits increases in device operating range which can be substantial. It is thus imperative that accurate thermal analysis and prediction be made available to maximize the utility of a bipolar transistor in a given system.

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