NON-ITERATIVE TECHNIQUE FOR COMPUTING TEMPERATURE DISTRIBUTIONS IN FLAT PLATES WITH DISTRIBUTED HEAT SOURCES AND CONVECTIVE COOLING

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ABSTRACT

An analytical/numerical model is presented for determining wall temperature distributions in PCB's due to heat conduction within the board. The analytical nature of the model allows thermal enhancement options such as material selection and component location to be readily assessed while requiring only modest computing capabilities such as a personal computer.

Several examples are presented to show the sensitivity of the model to changes in the thermal conductivity, the thickness of the PCB and the film coefficient due to forced convection.

NOMENCLATURE

A	- cross sectional area, m^2
Bi	- Biot number, ht/k_s
C_1, C_2, etc.	- constants of integration
h	- film coefficient, W/m^2K
k	- thermal conductivity, W/mK
ℓ	- element length, m
m	- parameter defined by Eqn. 20
n	- parameter defined by Eqns. 21 and 22
N	- total number of elements
q	- heat flux, W/m^2
Q	- total heat flow, W
t	- plate thickness, m
T	- temperature, K

Greek Symbols

β	- parameter defined by Eqn. 41
Λ	- parameter defined by Eqn. 42
K	- thermal conductivity ratio
ϑ	- temperature excess, K

Subscripts

cond	- conduction
conv	- convection
f_1	- fluid above the plate
f_0	- fluid below the plate
s	- solid
tot	- total
0	- below the plate
1	- above the plate

Superscripts

+	- as in Eqn. 40

INTRODUCTION

The extensive use of surface mount technology in today's printed circuit boards (PCB's) has allowed circuit designers to significantly increase component packing densities. This increased packing density combined with the use of higher powered device packages dissipating up to 7 W [Bergles, 1986] can lead to heat flux densities which approach 10,000 W/m^2. Localized temperatures on the surface of a PCB can exceed 125°C with device junction temperatures far exceeding reliable operating limits. The circuit designer is forced to make use of some form of thermal enhancement ranging from the use of secondary fluids in extreme overheating situations to the use of cooling fins for less serious overheating. Both of these forms of thermal enhancement often necessitate major design modifications which delays delivery and radically increases production costs. For applications where junction temperatures marginally exceed recommended operating temperatures, the circuit designer has several thermal enhancement options available, including fundamental design improvements by optimizing the use of available PCB materials and laying out the board in a thermally optimum manner. This approach can significantly reduce the major design changes as previously mentioned; however, it is dependent upon the availability of a model which is accurate and requires minimal learning and setup time.

Several investigators [Eckert et al, 1957; Ling, 1963; Reynolds et al, 1958; Sogin, 1960] have developed analytical techniques for predicting temperatures on flat plates with either an isothermal or a nonisothermal condition imposed at the surface. However, these

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solution techniques are based solely on fluid side heat transfer, choosing to ignore heat conduction into the substrate. This assumption can lead to a significant over estimation of peak board temperatures depending on the geometry and the thermophysical properties of the application.

Other solutions [Atsugi et al, 1969 and Pinto et al, 1986] to the problem of multi-dimensional steady conduction within a flat plate have been developed primarily based on finite difference and finite element techniques. These analyses provide accurate and detailed information; however, the computing requirements often prohibit their use as an everyday design aid.

A careful examination of typical thermophysical properties and board dimensions indicates that complex two and three dimensional heat transfer analyses are not always necessary to predict circuit board temperatures accurately. The principal objective of this paper is to develop a general analytical/numerical solution technique for predicting surface temperatures on PCB's populated with any number of arbitrarily located components. Since actual circuit boards rarely perform as idealized flat plates with heat sources having uniformly distributed heat flux, a model should allow the heat source flux distribution to be specified in an arbitrary manner. Similarly, the film coefficient is rarely uniformly distributed, therefore the model should allow for arbitrary distributions.

The sensitivity of plate temperature with respect to flow conditions and various thermophysical properties will be examined using the proposed model as described above. Only those properties over which the circuit designer has some control will be studied in detail. This parametric study will give some insight into the relative merit of varying one parameter in relation to others.

MODEL DEVELOPMENT

For analytical analysis it is convenient to section the circuit board into two distinct regions, areas which are populated with heat generating devices such as IC packages and areas which are free of heat sources. For the purpose of this paper these areas will be referred to as source and non-source sections respectively. If the components on the surface of the circuit board are assumed continuous in the y direction, the thermal interaction perpendicular to the air flow direction can be neglected and the idealized cross section of the circuit board in the axial direction would look similar to the schematic shown in Fig. 1.

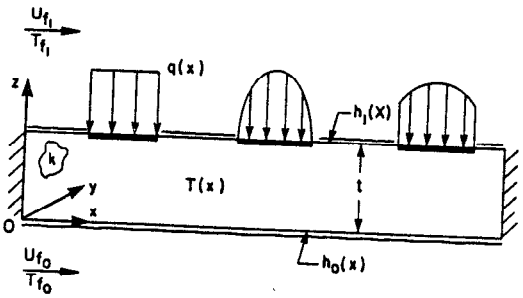

Figure 1. Idealized Cross Section of a Circuit Board

As seen from Fig. 1, further simplifying assumptions have be made, notably the heat sources are considered to be flush mount with the surface of the circuit board, the contact resistance betwe the source and the circuit board is considered to be negligible and t. leading and trailing edge of the plate are adiabatic. Source regio can be characterized by a total power dissipation, which in the ca. of an IC package will be the heat dissipated at the surface of the d As a further simplifying assumption the heat transferred from t. top of the device package by means of radiation and convection w be lumped as a single outward directed heat flow denoted as Q_{con} Similarly, the heat conducted through the leads or convected off th back side of the device package will be lumped as a single inwar directed heat flow denoted as Q_{cond} as shown in Fig. 2.

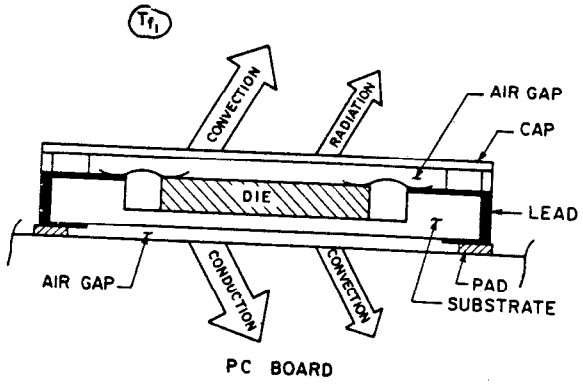

Figure 2. Heat Flow from an IC Package

The total power dissipated by a source in the form of heat can be written as

$$Q_{tot} = Q_{conv} + Q_{cond} \tag{1}$$

If the heat transfer area is considered constant for each component of heat flow Eqn. 1 can then be written as

$$q_{tot} = q_{conv} + q_{cond} \tag{2}$$

where q_{tot} is the total heat generation of the heat source.

Governing Equation

The governing equation for heat conduction within a solid is Laplace's equation, which in two dimensions is given as

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial z^2} = 0 \tag{3}$$

If the cross sectional dimensions are assumed constant, the temperature over any yz plane can be determined by integrating Eqn. 3 over the thickness of the board from $z = 0$ to $z = t$.

$$\int_0^t \frac{\partial^2 T}{\partial x^2} dz + \int_0^t \frac{\partial^2 T}{\partial z^2} dz = 0 \tag{4}$$

The second term in Eqn. 4 can be directly integrated to give

$$\int_0^t \frac{\partial^2 T}{\partial z^2} dz = \left.\frac{\partial T}{\partial z}\right|_{z=t} - \left.\frac{\partial T}{\partial z}\right|_{z=0} \tag{5}$$

Using Leibnitz rule the first term in Eqn. 4 can be rewritten as

$$\int_0^t \frac{\partial^2 T}{\partial x^2} dz = \frac{\partial^2}{\partial x^2}\left[\int_0^t T dz\right] = t\frac{\partial^2 \bar{T}}{\partial x^2} \tag{6}$$

where $\bar{T}$ the mean temperature over the thickness is given by

$$\bar{T} = \frac{1}{t}\int_0^t T\,dz \tag{7}$$

d the board thickness is assumed to be constant with respect to x. Substituting Eqns. 5 and 6 into Eqn. 4 gives

$$\frac{\partial^2 \bar{T}}{\partial x^2} + \frac{1}{t}\left.\frac{\partial T}{\partial z}\right|_{z=t} - \frac{1}{t}\left.\frac{\partial T}{\partial z}\right|_{z=0} = 0 \tag{8}$$

Eqn. 8 can then be solved for temperature, subject to the boundary conditions imposed at the solid/fluid interface.

Boundary Conditions

Top Surface

The top surface of the circuit board consists of both source and non-source sections, therefore, the boundary conditions on this surface must vary subject to local conditions. A Neumann boundary condition as given in Eqn. 9 is specified at the source sections.

$$\left.\frac{\partial T}{\partial z}\right|_{z=t} = \frac{q_{cond}}{k_s} \tag{9}$$

From Eqn. 2, Eqn. 9 can then be written as

$$\left.\frac{\partial T}{\partial z}\right|_{z=t} = \frac{q_{tot} - q_{conv}}{k_s} \tag{10}$$

where

$$q_{conv} = h_1(T_{(z=t)} - T_{f_1}) \tag{11}$$

The source boundary condition then becomes

$$\left.\frac{\partial T}{\partial z}\right|_{z=t} = \frac{q_{tot} - h_1(T_{(z=t)} - T_{f_1})}{k_s} \tag{12}$$

A Robin boundary condition is specified at all non-source locations.

$$\left.\frac{\partial T}{\partial z}\right|_{z=t} = -\frac{h_1}{k_s}(T_{(z=t)} - T_{f_1}) \tag{13}$$

Bottom Surface

A Robin boundary condition is specified over the bottom surface of the board both for source and non-source sections. Because of the choice of positive z in the upward direction the boundary condition given in Eqn. 14 has a sign change from that of Eqn. 13.

$$\left.\frac{\partial T}{\partial z}\right|_{z=0} = \frac{h_0}{k_s}(T_{(z=0)} - T_{f_0}) \tag{14}$$

The boundary conditions in Eqns. 12, 13 and 14 can then be used to solve for temperature in Eqn. 8.

Board Temperature Solution

The temperature gradient across the thickness of the board is typically small given the dimensions and the thermophysical properties of most circuit boards, i.e. $Bi = ht/k_s < 0.1$. Consequently, the temperature at the upper and lower surface of the circuit board can be assumed to be identical.

$$T_{(z=0)} = T_{(z=t)} = \bar{T} \tag{15}$$

and the temperature excess is given by

$$\vartheta = \bar{T} - T_{f_1} \tag{16}$$

By substituting Eqns. 12 – 14 and Eqn. 16 into Eqn. 8 the governing differential equations for the source and non-source sections become

Source

$$\frac{\partial^2 \vartheta}{\partial x^2} - \left[\frac{h_0 + h_1}{k_s t}\right]\vartheta = -\left[\frac{q_{tot} + h_0(T_{f_o} - T_{f_1})}{k_s t}\right] \tag{17}$$

Non-Source

$$\frac{\partial^2 \vartheta}{\partial x^2} - \left[\frac{h_0 + h_1}{k_s t}\right]\vartheta = -\left[\frac{h_0(T_{f_0} - T_{f_1})}{k_s t}\right] \tag{18}$$

Solving for ϑ in Eqns. 17 and 18 gives

$$\vartheta(x) = C_1\, e^{-mx} + C_2\, e^{mx} + \frac{n}{m^2} \tag{19}$$

where,

$$m^2 = \frac{h_o + h_1}{k_s t} \tag{20}$$

and

$$n = \frac{q_{tot} + h_0(T_{f_0} - T_{f_1})}{k_s t}, \qquad \text{(source)} \tag{21}$$

or

$$n = \frac{h_0(T_{f_0} - T_{f_1})}{k_s t}, \qquad \text{(non-source)} \tag{22}$$

Constants of Integration

The constants of integration can be determined for each section over the length of the plate by imposing two boundary conditions at the common interface between each section as shown in Fig. 3.

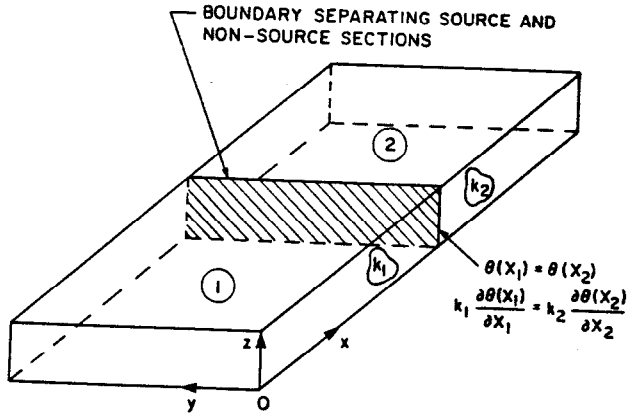

Figure 3. Section Coupling Boundary Conditions

The first boundary condition is a consequence of the assumption that there is perfect contact between each section. As a result the temperature excess immediately adjacent to either side of the interface will be identical and

$$\vartheta(x_i) = \vartheta(x_{i+1}) \tag{23}$$

The second boundary condition can be obtained by using the principle of conservation of energy across the interface.

$$Q_i = Q_{i+1}$$

$$-k_i A\frac{\partial \vartheta(x_i)}{\partial x_i} = -k_{i+1}A\frac{\partial \vartheta(x_{i+1})}{\partial x_{i+1}}$$

$$k_i \frac{\partial \vartheta(x_i)}{\partial x_i} = k_{i+1} \frac{\partial \vartheta(x_{i+1})}{\partial x_{i+1}} \quad (24)$$

Based on the previous assumption that the leading and trailing edges of the board are adiabatic, the boundary condition at these faces will be

$$\frac{\partial \vartheta(x_i)}{\partial x_i} = 0 \quad (25)$$

By substituting Eqns. 20 – 25 into Eqn. 19, a series of equations will be obtained which can be solved using conventional matrix solving techniques such as Gaussian elimination. However, in some instances these methods can be computationally intensive making them prohibitive when analysing circuit boards with many heat sources. The method chosen to determine the constants of integration involves solving for a single constant of integration at the leading edge of the board which can then be used to obtain all other constants through linear combinations of the leading edge constant.

A standard circuit board will be assumed to have a non-source section at the leading and trailing edge with alternating source and non-source sections in between.

A board with N discrete sections necessitates solving for $2N$ constants of integration and therefore $2N$ equations must be solved simultaneously. Substituting Eqns. 20 – 25 into Eqn. 19 and equating common terms at matching interfaces the following equations are obtained:

$$C_1 = C_2 \quad (26)$$

$$C_3 + C_4 + \frac{n_2}{m_2^2} = C_1 e^{m_1 \ell_1} + C_2 e^{m_1 \ell_1} + \frac{n_1}{m_1^2} \quad (27)$$

$$-m_2 C_3 + m_2 C_4 = -K_1 m_1 C_2 e^{m_1 \ell_1} K_1 m_1 C_2 e^{m_1 \ell_1} \quad (28)$$

$$C_5 + C_6 + \frac{n_3}{m_3^2} = C_3 e^{-m_2 \ell_2} + C_4 e^{m_2 \ell_2} + \frac{n_2}{m_2^2} \quad (29)$$

$$-m_3 C_5 + m_2 C_6 = -K_2 m_2 C_3 e^{-m_2 \ell_2} + K_2 m_2 C_4 e^{m_2 \ell_2} \quad (30)$$

$$\vdots$$

$$C_{(2N-1)} + C_{(2N)} + \frac{n_N}{m_N^2} = C_{(2N-3)} e^{-m_{N-1} \ell_{N-1}} + C_{(2N-2)} e^{m_{N-1} \ell_{N-1}} + \frac{n_{N-1}}{m_{N-1}^2} \quad (31)$$

$$-m_N C_{(2N-1)} + m_N C_{(2N)} = -K_{N-1} M_{N-1} C_{(2N-3)} e^{m_{N-1} \ell_{N-1}} + K_{N-1} m_{N-1} C_{(2N-2)} e^{-m_{N-1} \ell_{N-1}} \quad (32)$$

$$C_{(2N-1)} = C_{(2N)} e^{2 m_N \ell_N} \quad (33)$$

where the conductivity ratio is given by

$$K_i = \frac{k_i}{k_{i+1}}. \quad (34)$$

Through a method of substituting Eqn. 33 into Eqns. 31 and 32 and successively substituting into Eqns. 30 through 26, C_1 can be determined in terms of known basic design information such as section length (ℓ), source heat flux (q_{tot}), film coefficient (h) and the thermal conductivity of the circuit board(k_s). The leading edge constant of integration is given as

$$C_1 = \frac{n_N}{m_N^2} \left\{ \frac{\Lambda_N^+}{2 \Pi_{i=1}^N \Lambda_i^+} \right\} + \sum_{i=2}^{N-1} \frac{n_i}{m_i^2} \left\{ \frac{\Lambda_i^+ - 1}{2 \Pi_{i=1}^N \Lambda_i^+} \right\} + \frac{n_1}{m_1^2} \left\{ \frac{-1}{2 \Lambda_1^+} \right\} \quad (35)$$

where

$$n_i = \frac{(h_0)_i (T_{f_o} - T_{f_i})}{k_i t}, \quad \text{(non-source)} \quad (36)$$

$$n_i = \frac{q_i + [(h_0)_i (T_{f_o} - T_{f_i})]}{k_i t}, \quad \text{(source)} \quad (37)$$

$$m_i^2 = \frac{(h_0)_i + (h_1)_i}{k_i t} \quad (38)$$

where i is the element designation, with the leading edge non-source element being 1st element, and the trailing edge non-source element being Nth element.

$$\Lambda_i^+ = \frac{\beta_i e^{m_i \ell_i}}{\Lambda_{i+1}} \quad (39)$$

$$= (\beta_i) \sinh(m_i \ell_i) + \cosh(m_i \ell_i) \quad (40)$$

$$\beta_i = K_i \frac{m_i \Lambda_{i+1}}{m_{i+1}}, \qquad i < n \quad (41)$$

$$\Lambda_i = \frac{(\beta_i) \cosh(m_i \ell_i) + \sinh(m_i \ell_i)}{(\beta_i) \sinh(m_i \ell_i) + \cosh(m_i \ell_i)}, \qquad i < n \quad (42)$$

$$\Lambda_N = \coth(m_N \ell_N) \quad (43)$$

A typical calculation procedure for determining the constants of integration would be as follows:

1. determine Λ_N, knowing m_N and ℓ_N
2. determine β_{N-1}, knowing Λ_N, m_N, m_{N-1}, and K_{N-1}
3. determine Λ_{N-1} and Λ_{N-1}^+
4. determine the remaining Λ_i 's, β_i 's and Λ_i^+ 's
5. calculate C_1

The remaining constants of integration can be determined for each source and non-source section by using the general form of C_{2i-1} and C_{2i} as given in Eqns. 45 and 46.

$$C_2 = C_1 \quad (44)$$

for i=2 to N

$$C_{2i-1} = .5 \left\{ C_{i-1} e^{-m_{i-1} \ell_{i-1}} \left(1 + K_{i-1} \frac{m_{i-1}}{m_i} \right) + C_{2(i-1)} e^{m_{i-1} \ell_{i-1}} \left(1 - K_{i-1} \frac{m_{i-1}}{m_i} \right) + \left(\frac{n_{i-1}}{m_{i-1}^2} - \frac{n_i}{m_i^2} \right) \right\} \quad (45)$$

$$C_{2i} = .5 \left\{ C_{i-1} e^{-m_{i-1} \ell_{i-1}} \left(1 - K_{i-1} \frac{m_{i-1}}{m_i} \right) + C_{2(i-1)} e^{m_{i-1} \ell_{i-1}} \left(1 + K_{i-1} \frac{m_{i-1}}{m_i} \right) + \left(\frac{n_{i-1}}{m_{i-1}^2} - \frac{n_i}{m_i^2} \right) \right\} \quad (46)$$

The board temperature at any location within each discretized element can be obtained from

$$\vartheta(x_i) = C_{2i-1}\, e^{-m_i x_i} + C_{2i}\, e^{m_i x_i} + \frac{n_i}{m_i^2} \qquad (47)$$

MODEL ANALYSIS

Most practical applications involving distributed heat sources arbitrarily located on a flat plate rarely conform to classic text book solution techniques where the heat flux is uniformly distributed over the sources. A more representative heat flux distribution over a microelectric device package, as shown through infra-red photography[1], is a parabolic distribution with the peak heat flux occurring in the center of the package. Three step change heat flux distributions as shown in Fig. 4, ranging from a crude approximation of a parabolic distribution given as a uniform heat flux over the full source, to a distribution consisting of 100 step changes which closely approximates a true parabolic distribution are examined to observe the effect of heat flux distribution on peak source temperature. The relative difference in peak source temperature in Fig. 5 is defined as

$$\left\{\begin{array}{c}\text{Relative Diff.}\\ \text{in}\\ \text{Peak Temp.}\end{array}\right\} = \frac{\left\{\begin{array}{l}\text{Peak Temp. with}\\ \text{Parabolic Flux}\\ \text{Distribution}\end{array}\right\} - \left\{\begin{array}{l}\text{Peak Temp. with}\\ \text{Another Flux}\\ \text{Distribution}\end{array}\right\}}{\left\{\begin{array}{l}\text{Peak Temp. with}\\ \text{Parabolic Flux}\\ \text{Distribution}\end{array}\right\}}$$

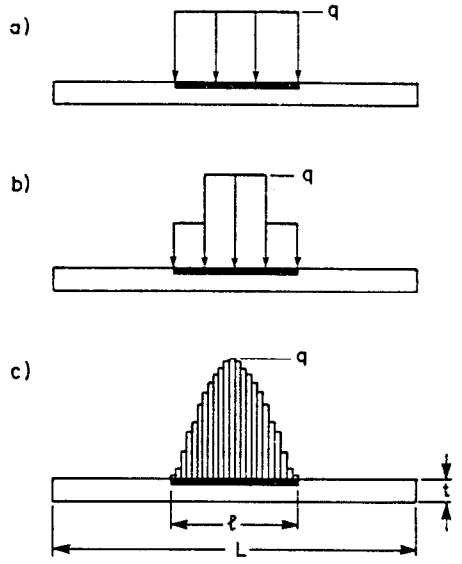

Figure 4. Heat Flux Distributions
a) uniform, b) 4 elements, c) 100 elements

As shown in Fig. 5, a uniform heat flux distribution underestimates peak source temperature by as much as 22 percent, depending on the size of the heat source in relation to the total length of the plate. Using a heat flux distribution characterized by four elements introduces a maximum error of slightly less than 5 percent, while the distribution using 100 elements gives a peak source temperature identical to the parabolic distribution. Conventional analytic solution techniques restricted to uniform distributions can lead to a significant underestimation of peak temperatures, however, a model which allows for even a coarse distribution with three or four elements per source can provide temperature predictions which are more in line with actual device temperatures.

[1]Personal Communications with Northern Telecom Ltd., Ottawa, Ontario.

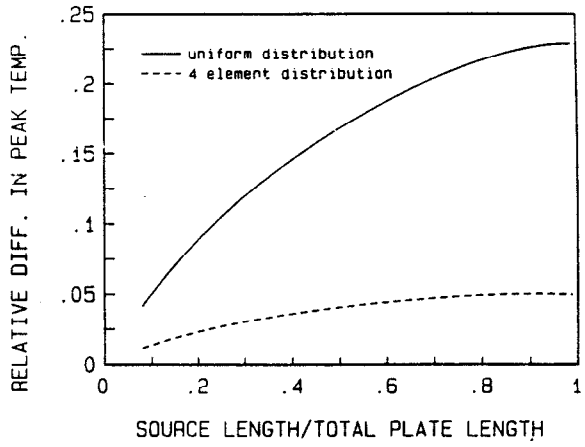

Figure 5. Effect of Heat Flux Distribution on Peak Temperature

DISCUSSION

During the initial stages of PCB design the circuit board designer is given some degree of freedom in selecting component materials and system operating conditions as long as certain electrical constraints are adhered to. However, there are only a limited number of design parameters which can be modified without disrupting the structural or electrical integrity of the board or causing manufacturing cost to escalate rapidly. Some of the design parameters which can be modified over a limited range include the thermal conductivity of the board, the board thickness and the flow velocity of the cooling medium. The effect these parameters have on peak board temperature will be examined in the following section.

The analysis of heat conduction within a substrate having distributed heat sources separated by convectively cooled regions can be very complex because of the difficulty in simplifying the problem by isolating a typical cell bounded by planes of symmetry. This necessitates using a technique which considers the thermal interaction between all heat sources, simultaneously. Analytical techniques on their own are not general enough to deal with the variety of boundary conditions which can be encountered in a problem of this nature. The thickness to board length aspect ratio for a typical circuit board exceeds 100:1. Most numerical techniques require many discrete elements to obtain meaningful results for a problem with this geometry. The cost of running numerical codes for such a problem generally limits their use in most microelectronic applications. The analytical/numerical technique presented here overcomes both of these shortcomings of the purely analytical or numerical techniques. The procedure is easy to code and typically requires less than one minute to solve a multiple heat source problem using an IBM–PC. Although the technique presented here allows for distributed sources with an arbitrarily distributed heat flux for each source or an arbitrarily distributed film coefficient, the examples presented in the following will be simplified for presentation clarity. A single heat source centrally located on a homogeneous substrate will be examined using the design information given in Table 1.

The film coefficient is assumed to be uniform over the front and back surface of the circuit board. A value of 20 W/m^2K is typical of a film coefficient observed over a circuit board cooled by laminar air flow at approximately 20°C. A board thermal conductivity of 5 W/mK is representative of a typical fiberglass board with copper tracking. The size and location of the heat source have been

total board length	-	0.15 m
board thickness	-	0.002 m
heat source length	-	0.05 m
heat source center	-	0.075 m
peak heat flux	-	3000 W/m^2
heat flux distribution	-	parabolic
film coefficient	-	20 W/m^{2}K
board thermal conductivity	-	5 W/mK

Table 1. Default Circuit Board Configuration

chosen to represent a lumped total of all heat sources that might appear on a typically sized circuit board. The modelling technique detailed above is capable of predicting surface temperatures for the distributed source problem, however the presentation of the results would not clearly show the effect of design changes on surface temperatures. The lumped source example more clearly shows the effect of thermophysical properties and flow conditions.

The data for each set of curves is obtained by varying only the parameter of interest, i.e. thermal conductivity, board thickness and film coefficient, while maintaining all other design parameters at the default value. The effect on surface temperature distribution is observed in each case. Temperature excess is defined as the difference between the wall temperature and some reference temperature, in this instance, the free stream temperature.

a) Board Thermal Conductivity

The thermal conductivity of the board plays a major role in the thermal spreading effect in the vicinity of the heat source. As shown in Fig. 5 the peak heat source temperature is strongly affected by the thermal conductivity of the board. The most significant reduction in peak heat source temperature occurs between a thermal conductivity of 1 and 10 W/mK, where a tenfold increase in thermal conductivity results in a 50% reduction in peak heat source temperature. Coincidentally, this is the range of board thermal conductivities observed in most fiberglass/copper PCB's. A small increase in copper content could significantly reduce the temperature at the heat source. Increasing the board thermal conductivity beyond 25 W/mK leads to a minimal reduction in peak source temperature since the board is approaching an isothermal condition beyond which increases in thermal conductivivty have little effect on board temperatures.

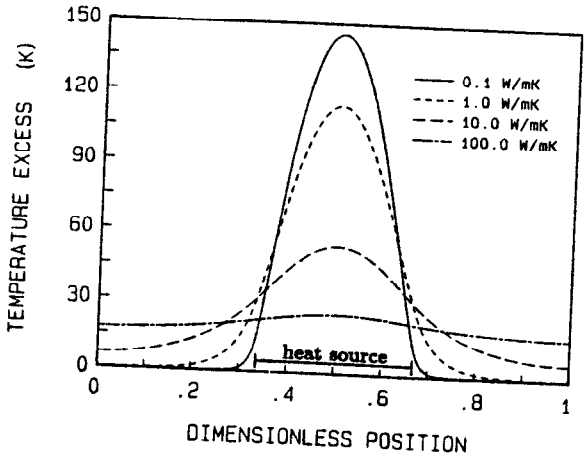

Figure 5. Effect of Board Thermal Conductivity on Temperature Excess

b) Board Thickness

A typical single layer board has a thickness of slightly less than 2 mm, while some multilayer boards may approach a thickness of 3mm. The effect on surface temperature due to varying thickness over this range of values is shown in Fig. 6.

A change in the thickness of the board has a similar effect on peak heat source temperature as was evident with changes in thermal conductivity. An increase in board thickness results in a decrease in peak heat source temperature as heat is distributed over a broader area about the heat source. Over the range of board thicknesses examined the decrease in peak source temperature is approximately inversely proportional to the square root of the change in board thickness. A 100% increase in board thickness from 1 to 2 mm reduces the peak temperature by approximately 20%. Similarly, an increase in board thickness from 2 – 4 mm results in a 20% decrease in peak temperature.

The circuit designer rarely increases the thickness of the circuit board as a method of improving heat conduction. A copper ground plane may sometimes be added and the board thickness increases, however it is principally the increase in effective thermal conductivity due to the higher copper content which improves heat conduction.

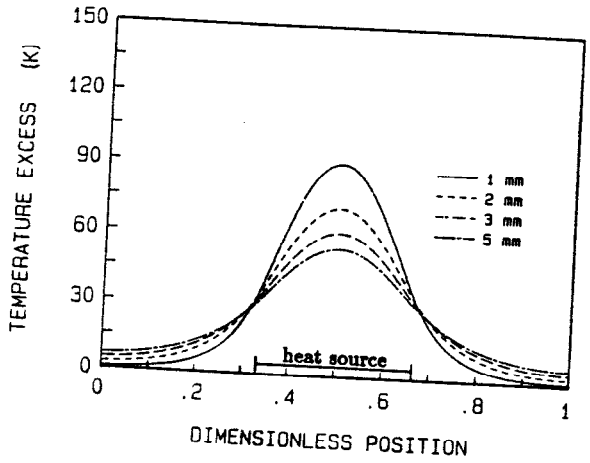

Figure 6. Effect of Board Thickness on Temperature Excess

c) Film Coefficient

The resistance to heat flow ($R = 1/hA$) at the surface of a PCB is a function of the flow conditions imposed on both sides of the board. In particular, the film coefficient (h), varies as a function of the square root of the flow velocity in laminar flow. For the purpose of this study temperature excess is plotted versus the film coefficient, however temperature excess could be plotted versus flow velocity.

Fig. 7 shows the effect on surface temperature due to a change in a uniformly distributed film coefficient. The most significant reduction in peak temperature occurs for an increase in film coefficient from 10 to 30 W/m^{2}K. A film coefficient of this order can be easily obtained with the use of small, low cost axial fans producing flow velocities of 1 – 3 m/s. This is particularly noteworthy for a designer considering using forced convection for an application which has previously relied on free convection. Increases in the film coefficient above 30 W/mK provide only a moderate reduction in peak temperature while requiring the designer to use a costly and often noisy centrifugal blower.

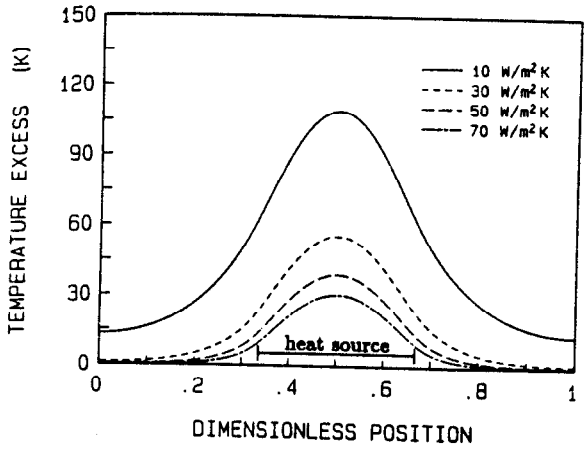

Figure 7. Effect of Film Coefficient on Temperature Excess

SUMMARY AND CONCLUSIONS

1. The use of simple modelling tools which allow for only a uniform heat flux or film coefficient distribution can lead to significant errors in predicting peak board temperatures.

2. The thermal conductivity of the board is the sole most important design parameter for reducing board temperatures. A marginal increase in the relative percentage of copper within a board will result in an increased effective thermal conductivity and can lead to significant reduction in board temperature especially when the effective thermal conductivity of the board is between 1 and 10 W/mK.

3. An increase in the free stream flow velocity and in turn the film coefficient is an effective means of reducing peak board temperatures especially for film coefficients of 30 W/m^2K and less.

4. The circuit designer may alter the thickness of the circuit board by only a fraction of a millimetre. The resulting effect on board temperatures is not sufficient to warrant changing the design of the board.

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