THERMAL ANALYSIS AND OPTIMIZATION OF CONVECTIVELY-COOLED MICROELECTRONIC CIRCUIT BOARDS

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ABSTRACT

An approximate analytical solution to a fundamental basis problem for heat conduction in a convectively-cooled microelectronic circuit board has been derived by employing a novel approach for treating mixed boundary conditions. Results obtained with this solution indicate that increasing the chip spacing decreases the thermal resistance of the circuit board for many cooling configurations only if accompanied by an increased board thickness. Thus in many practical applications, little gain in thermal performance of the board is realized for chip center-to-center spacings greater than twice the chip width. In addition, the analytical solution has also been used to estimate the accuracy of the compound-fin model for one-dimensional steady heat conduction in a microelectronic circuit board.

NOMENCLATURE

a	- half-width of IC chip
A_n	- series coefficient
b	- half of the IC chip center-to-center spacing
Bi_1, Bi_2	- Biot numbers ($Bi \equiv ht/k$) for the top and bottom surfaces of the circuit board respectively
C_{mn}	- entries in coefficient matrix (Eqs. (25) or (A-1))
E	- integral of errors squared in Eq. (17)
$g(\xi)$	- function for non-homogeneous boundary condition (Eq. (19))
G_n	- entries in right-hand side vector (Eqs. (26) or (A-5))
h_1, h_2	- convective heat transfer coefficients for the top and bottom surfaces of the circuit board respectively
h_{e1}, h_{e2}	- effective heat transfer coefficients for the top and bottom surfaces of the IC chip respectively
k	- homogeneous thermal conductivity
L	- length of IC chip(s) into the circuit board
m,n	- series solution indices
N	- number of series coefficients
q	- uniform heat flux
Q_1, Q_2	- total heat flow rates across top and bottom surfaces of the IC chip respectively
R_2	- thermal resistance of heat flow path into the circuit board
t	- thickness of the circuit board
T	- temperature
$\bar{T}_c$	- average temperature rise on contact between IC chip and circuit board
T_∞	- free-stream cooling fluid temperature
x,y,z	- Cartesian coordinate system

Greek Symbols

α	- aspect ratio of the board ($\equiv t/b$)
γ_3, γ_4	- dimensionless constants defined by Eqs. (14) and (A-4) respectively
δ_{mn}	- Kronecker delta function ($\delta_{mn}=0$ for $m \neq n$, $\delta_{mn}=1$ for $m=n$)
Δ_{mn}	- function used to evaluate C_{mn} (Eq. (A-2))
ε	- relative contact size ($\equiv a/b$)
η, ξ	- dimensionless coordinate system ($\xi \equiv x/b$, $\eta \equiv z/b$)
Λ_n	- function of Bi_1 and ε (Eq. (13))
τ_n	- function used to evaluate C_{mn} (Eq. (A-3))
$\phi_n(\xi)$	- functions for non-homogeneous boundary condition (Eq. (18))
ψ	- dimensionless resistance of fundamental basis problem ($\equiv k L R$) given by Eq. (31)
ψ_{CF}	- dimensionless resistance estimated from compound-fin model (Eqs. (35) or (40))
ψ^*_{CF}	- dimensionless resistance estimated from modified compound-fin model (Eq. (43))

Subscripts

m,n - refers to the series solution
1,2 - refers to the top and bottom surfaces respectively

INTRODUCTION

The present trend towards increasing power densities in modern integrated circuits requires a greater emphasis on thermal considerations in microelectronics packaging. If the simple and relatively economical air cooling scheme illustrated in Fig. 1 continues to be employed, it becomes imperative that the thermal resistance of this configuration be minimized. This goal can be achieved both by maximizing the convective heat transfer rates and by optimizing the circuit board layout for a given air cooling situation.

As shown in Fig. 2, the heat generated within a typical integrated circuit chip on a printed circuit board is removed through two main heat flow paths. The thermal resistance of the heat flow path Q_1 through the top of the chip can be minimized both by lowering the thermal resistance between the semiconductor devices and the top surface of the chip and by maximizing the effective heat transfer rates from the top surface of the chip. This latter goal might be achieved by the use of either extended surfaces (i.e. external fins) or enhanced convective cooling (i.e. turbulence generators). The thermal resistance of the second major heat flow path Q_2 shown in Fig. 2 can be minimized by lowering the thermal resistance between the semiconductor devices and the bottom casing of the chip, by providing a good contact or heat conduction path between the bottom casing and

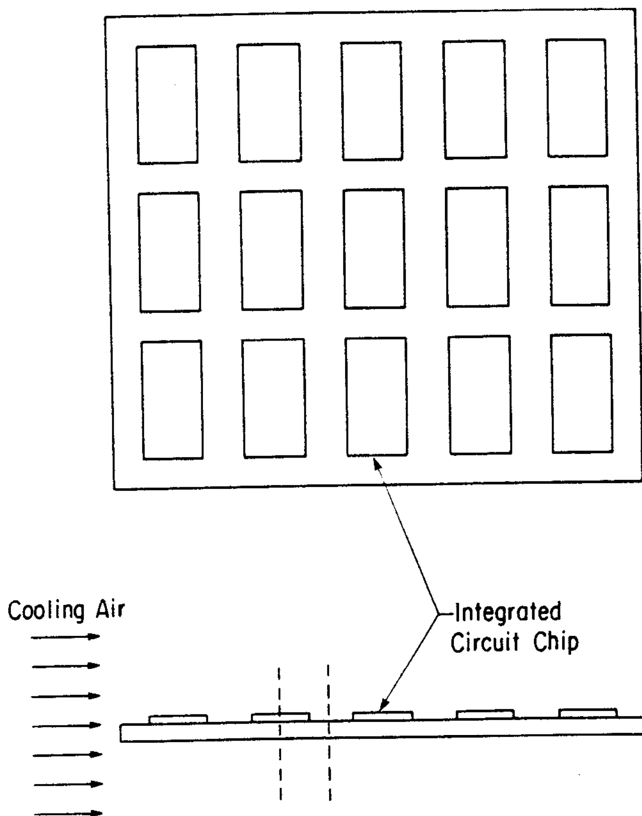

Fig. 1 Air Cooling of Integrated Circuit Chips on a Microelectronic Circuit Board

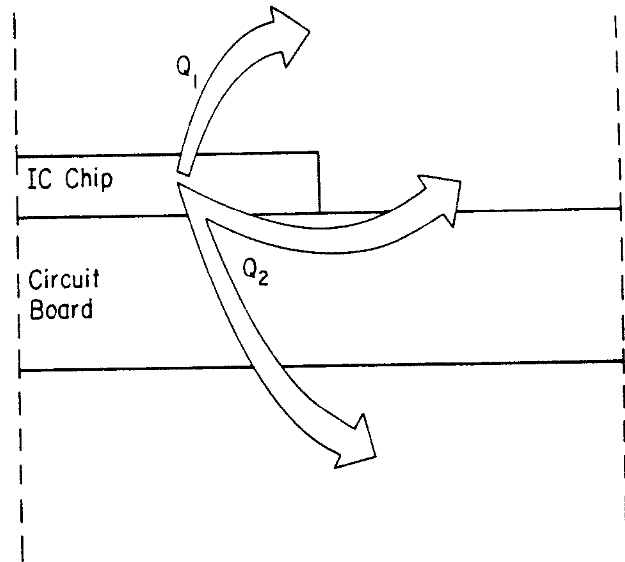

Fig. 2 Main Heat Flow Paths from an Integrated Circuit Chip

circuit board, and by optimizing the circuit board configuration for a given air cooling arrangement.

These two main heat flow paths are, in reality, coupled both by the interaction with the thermal-fluid boundary layer above the circuit board and by heat conduction within the integrated circuit chip. If, however, the physical approximation of modelling the two heat flow paths Q_1 and Q_2 as thermal resistances acting in parallel is made, then with the methods developed in this paper it can be shown that as much as 50% or even more of the total heat generation will flow through the bottom heat flow path Q_2 for typical circuit board layouts and little contact resistance (for example, surface-mount packaging). Therefore a tremendous motivation exists to optimize the circuit board configuration in an effort to reduce the overall thermal resistance of the cooling system and hence allow higher power densities for a given maximum device operating temperature. The development of an approximate analytical tool which can permit such an optimization for a given cooling scheme is then the first major goal of this work.

Accurate analysis of heat transfer due to air-cooling of a microelectronic circuit board is a complex task. In this paper only a fundamental basis problem for heat conduction in the circuit board is examined. This basis problem then allows relative comparisons of the thermal resistances for different circuit board layouts so that a designer can quickly select a configuration which best compromises the goals of minimal cost and minimal thermal resistance. The fundamental basis problem used to model circuit board heat conduction in this paper is shown in Fig. 3 where a uniform heat flux q enters a two-dimensional rectangular region with adiabatic ends and uniform heat transfer coefficients h_1 and h_2 on the top and bottom surfaces respectively. For convenience the free-stream temperature of the cooling air is taken as $T_\infty = 0$. The assumption of uniform heat transfer coefficients reflects both the fact that in most cases h_1 and h_2 can only be estimated roughly beforehand and that this selection simplifies the analysis. By assuming that a "large" number of similar integrated circuit chips are evenly distributed over the circuit board the conservative

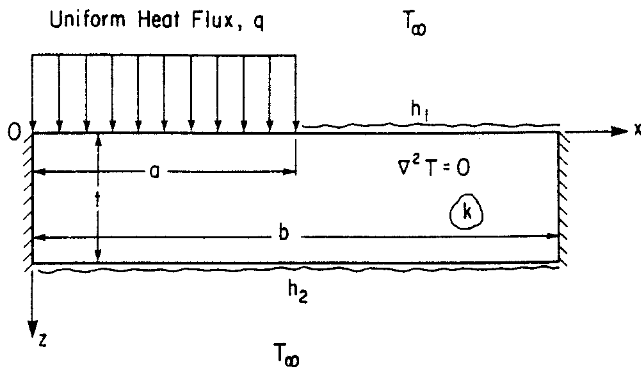

Fig. 3 Basis Problem for the Study of Thermal Resistance in a Microelectronic Circuit Board

(in terms of maximum temperature) assumption of adiabatic ends is chosen. Finally, prescribing a uniform heat flux into the circuit board allows objective comparisons of thermal resistance to be made only in terms of the parameters over which the designer has some direct control. Recent papers by Yovanovich (1976) and Negus and Yovanovich (1985) have also shown the relative insensitivity of thermal resistance to the exact form of the flux-specified boundary condition for complex heat conduction systems and that a uniform heat flux should give an upper bound on the true resistance of the board.

A more thorough analysis of heat transfer from integrated circuit chips on a printed circuit board requires a consideration of the coupling between the heat conduction in the circuit board and the behaviour of the thermal-fluid boundary layers surrounding the board (also known as the conjugate problem). In theory this entails a simultaneous solution of the momentum and energy equations in the cooling fluid and Laplace's equation in the board with potentially significant computational costs using standard numerical methods. However, a good approximate solution can be developed by combining integral boundary layer analysis with a one-dimensional or compound-fin model of heat conduction in the board as proposed by Culham (1985). Thus a second major goal of this paper is to examine the limits of the one-dimensional or compound-fin model for heat conduction under typical air-cooling conditions.

THEORETICAL DERIVATION

Under the assumptions of homogeneous, isotropic thermal conductivity k and steady-state conditions, heat conduction in the basis problem shown in Fig. 3 is governed by the following partial differential equation and boundary conditions:

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial z^2} = 0 \qquad (1)$$

$$\frac{\partial T}{\partial x}(0,z) = 0 \qquad (2)$$

$$\frac{\partial T}{\partial x}(b,z) = 0 \qquad (3)$$

$$k\frac{\partial T}{\partial z}(x,t) + h_2\, T(x,t) = 0 \qquad (4)$$

$$-k\frac{\partial T}{\partial z}(x,0) + h(x)T(x,0) = q(x) \qquad (5)$$

where

$$h(x) = \begin{cases} 0 \quad , & 0 \le x \le a \\ h_1 \quad , & a < x \le b \end{cases} \qquad (6)$$

$$q(x) = \begin{cases} q \quad , & 0 \le x \le a \\ 0 \quad , & a < x \le b \end{cases} \qquad (7)$$

The solution to this problem governed by Laplace's equation with consideration of the three homogeneous boundary conditions of Eqs. (2), (3) and (4) is determined in a straightforward manner using the separation of variables technique to yield

$$T(x,z) = \frac{qt}{k}\{D[1 - \frac{Bi_2\eta}{\alpha(Bi_2 + 1)}] + \sum_{n=1}^{\infty} A_n \cos n\pi\xi\ [\cosh n\pi\eta - \Omega_n \sinh n\pi\eta]\} \qquad (8)$$

where $\xi \equiv x/b$ and $\eta \equiv z/b$ represent dimensionless coordinates, the factor qt/k which has dimensions of temperature permits dimensionless constants D and A_n, and the Biot number on the bottom surface and aspect ratio of the board are defined respectively as

$$Bi_2 \equiv h_2 t/k \qquad (9)$$

$$\alpha \equiv t/b \qquad (10)$$

In addition,

$$\Omega_n = \frac{\alpha n\pi \tanh n\pi\alpha + Bi_2}{\alpha n\pi + Bi_2 \tanh n\pi\alpha} \qquad (11)$$

Unfortunately though, the classical method of separation of variables can not account for the mixed boundary condition of Eq. (5) which arises when h(x) of Eq. (6) varies on z=0 for $0 \le x \le b$. To overcome this restriction a special approximate analytical technique must be developed to determine the unknown series coefficients A_n in Eq. (8) from the non-homogeneous boundary condition of Eq. (5). This procedure is initiated by relating the constant D in Eq. (8) to the series coefficients by substituting Eq. (8) into Eq. (5) and simply integrating from x=0 to x=b to give

$$D = [\varepsilon - \sum_{n=1}^{\infty} A_n \Lambda_n]/\gamma_3 \qquad (12)$$

where

$$\Lambda_n = -Bi_1 \frac{\sin n\pi\varepsilon}{n\pi} \qquad (13)$$

$$\gamma_3 = Bi_2/(Bi_2+1) + Bi_1(1-\varepsilon) \qquad (14)$$

and the Biot number for the top surface and the relative contact size of the chip on the circuit board are defined respectively as

$$Bi_1 \equiv h_1 t/k \qquad (15)$$

$$\varepsilon \equiv a/b \qquad (16)$$

The unknown series coefficients A_n must now be determined by substituting Eqs. (12) and (8) into Eq. (5) and rearranging terms such that the non-homogeneous boundary condition is expressed by the relationship

$$\sum_{n=1}^{\infty} A_n \phi_n(\xi) = g(\xi) \qquad 0 \leq \xi \leq 1 \qquad (17)$$

where the functions $\phi_n(\xi)$ and $g(\xi)$ are

$$\phi_n(\xi)=\cos n\pi\xi \; [n\pi\Omega_n \alpha\gamma_3+Bi(\xi)\gamma_3]-\Lambda_n[\frac{Bi_2}{Bi_2+1}+Bi(\xi)] \qquad (18)$$

$$g(\xi) = \gamma_3\beta(\xi) - \varepsilon Bi(\xi) - \varepsilon \; Bi_2/(Bi_2+1) \qquad (19)$$

where

$$Bi(\xi) = \begin{cases} 0 \;, & 0 \leq \xi \leq \varepsilon \\ Bi_1 \;, & \varepsilon < \xi \leq 1 \end{cases} \qquad (20)$$

$$\beta(\xi) = \begin{cases} 1 \;, & 0 \leq \xi \leq \varepsilon \\ 0 \;, & \varepsilon < \xi \leq 1 \end{cases} \qquad (21)$$

In a classical separation of variables problem, the unknown series coefficients A_n would now be determined by invoking an orthogonality property of eigenfunctions $\phi_n(\xi)$ over the interval of the non-homogeneous boundary condition (Fourier's Method). However in this case the functions $\phi_n(\xi)$ of Eq. (18) are not orthogonal over the range $0 \leq \xi \leq 1$ because of the mixed boundary condition imposed on the top surface. Thus Fourier's Method cannot be applied to this problem and it would appear that a solution technique other than separation of variables should be utilized.

This is particularly frustrating because the solution obtained thus far satisfies both the governing partial differential equation and all of the homogeneous boundary conditions. A recent paper by Negus and Yovanovich (1984) has shown, at least for image methods applied to heat conduction, that excellent approximate solutions can be obtained by satisfying one or more boundary conditions only in a least-squares sense. This suggests that a finite number, N, of unknown series coefficients A_n might be determined by minimizing the continuous integral of errors squared in Eq. (17) defined as

$$E = \int_0^1 [g(\xi) - \sum_{n=1}^{N} A_n\phi_n(\xi)]^2 d\xi \qquad (22)$$

Minimization of E is effected by requiring that

$$\frac{\partial E}{\partial A_m} = 0 \qquad m=1,2,3, \ldots, N \qquad (23)$$

which then creates the system of linear algebraic equations

$$[C_{mn}]\{A_n\} = \{G_n\} \qquad (24)$$

from which the unknown series coefficients A_n can be determined. The entries in the coefficient matrix $[C_{mn}]$ and right-hand side vector $\{G_n\}$ are defined as

$$C_{mn} = \int_0^1 \phi_n(\xi)\phi_m(\xi)d\xi \qquad (25)$$

$$G_n = \int_0^1 g(\xi)\phi_n(\xi)d\xi \qquad (26)$$

and exact expressions for C_{mn} and G_n are contained in Appendix I.

An approximate solution for the temperature throughout the circuit board section of Fig. 3 is now available by combining Eq. (8) with the coefficients A_n found by solving the linear system of Eq. (24). Furthermore, Negus (1985) has recently proven mathematically that as $E \to 0$ (or the number of coefficients, N, becomes arbitrarily large) the approximate solution obtained uniformly approaches the exact solution everywhere in the solution domain. Thus any desired degree of accuracy for this approximate solution can be achieved, at least in theory, by increasing the number of series coefficients in the solution.

It is interesting to note that in the limiting case where the functions $\phi_n(\xi)$ are orthogonal on the range $0 \leq \xi \leq 1$ (i.e. no mixed boundary condition), the off-diagonal entries in $[C_{mn}]$ are zero and the series coefficients determined by this formulation are thus identical to those found by direct application of Fourier's Method. In practise it even appears that some "residual orthogonality" remains for the actual $\phi_n(\xi)$ functions in this problem as inspections of the matrices $[C_{mn}]$ produced by Eq. (25) clearly indicate significant diagonal dominance. Furthermore, it is also interesting to observe that the system of linear equations produced by this method of minimizing the integral of errors squared is identical to that which would result from direct application of Galerkin's Method in approximating the boundary condition of Eq. (17).

The thermal resistance, R_2, of the basis problem illustrated in Fig. 3 is given by the definition

$$R_2 = \frac{\bar{T}_c - T_\infty}{Q_2} \qquad (27)$$

where in this problem $T_\infty = 0$ and Q_2 is the total heat flow rate crossing the contact portion of the circuit board, or

$$Q_2 = q \; L \; a \qquad (28)$$

where L is the length of the chip into the plane of the paper in Fig. 3. The average temperature rise on the contact portion of the circuit board is defined as

$$\bar{T}_c = \frac{1}{a} \int_0^a T(x,0)dx \qquad (29)$$

Finally, a dimensionless thermal resistance parameter is introduced as

$$\psi \equiv k \; L \; R_2 \qquad (30)$$

The combination of Eqs. (8), (27), (28), (29)

and (30) then leads to the following approximate expression for ψ with N coefficients A_n determined by solving Eq. (24)

$$\psi \approx \frac{\alpha}{\varepsilon}\{[\varepsilon - \sum_{n=1}^{N} A_n\Lambda_n]/\gamma_3 + \frac{1}{\varepsilon}\sum_{n=1}^{N}\frac{A_n \sin n\pi\varepsilon}{n\pi}\} \quad (31)$$

OPTIMIZATION FOR SPECIFIC COOLING ARRANGEMENTS

The computation of the dimensionless thermal resistance as given by Eq. (31) requires the solution of Eq. (24) for some finite number of series coefficients A_n. Formulation of the system of equations is accomplished using the expressions given in Appendix I. These exact expressions for the matrix coefficients C_{mn} and G_n might appear somewhat formidable but are actually quite simple to implement in BASIC on a personal computer. An extremely efficient decomposition process is used to solve the resultant system of equations which are diagonal dominant. The symmetric property of $[C_{mn}]$ is also exploited to reduce both storage requirements and execution time. Up to 110 coefficients can be found by direct solution with compiled Microsoft BASIC on an IBM-PC with this limitation arising only from the 64 Kbyte maximum array space of this compiler.

Practical problems with convectively-cooled microelectronic circuit boards usually require anywhere from 10 to 200 coefficients to obtain accuracy better than 1% for ψ and typical execution times are under one minute. A somewhat larger number of coefficients are required to accurately compute the temperatures on the top surface although substantially fewer are needed to compute temperatures elsewhere. As might be expected from physical intuition, the case requiring the greatest number of coefficients occurs when the aspect ratio α is very small (a relatively thin board), the bottom surface is insulated ($h_2 = 0$), and the top surface has a high convective heat transfer coefficient h_1. When greater than 110 coefficients are required, the solution is still obtained using the IBM-PC but the coefficients are determined by block iteration. The system of equations given by Eq. (24) is ideally suited for block iterative techniques because of the diagonal dominance of $[C_{mn}]$ and because the A_n decrease in value as n increases (usually only 1 iteration is required).

The dimensionless thermal resistance parameter ψ derived in the previous section is a function of four dimensionless parameters or

$$\psi = \psi\,(\alpha, \varepsilon, Bi_1, Bi_2) \quad (32)$$

The aspect ratio α and the relative contact size ε describe the geometry of the board while the Biot numbers Bi_1 and Bi_2 reflect a combination of the convective-cooling arrangement, the thermal conductivity of the board, and the geometry. Ths use of these dimensionless groups reduces the number of unknowns in the basis problem of Fig. 3 from six (a, b, t, k, h_1, h_2) to four. Nonetheless, these four independent parameters can vary over wide ranges of values which makes it simply unfeasible to present extensive results in a paper of finite length.

Presentation of graphical results is greatly simplified by considering only the often-encountered case for forced-air cooling where top and bottom heat transfer coefficients are approximately identical, or $Bi_1 \approx Bi_2$. Example graphical results are shown in Figs. 4 and 5 where the dimensionless resistance ψ is plotted against α and ε for the fixed Biot numbers $Bi_1 = Bi_2 = .01$ and $Bi_2 = Bi = .1$.

A comparison of Figs. 4 and 5 shows that for similar geometry, an increase in the Biot number from .01 to .1 causes a substantial reduction in the thermal resistance of the board. However, changes in thermal resistance which result from different geometrical configurations are much more difficult to interpret from plots such as Figs. 4 and 5. For example, consider a case where $\alpha = .05$, $\varepsilon = .4$ and $Bi_1 = Bi_2 = .01$ (see Fig. 4). If the aspect ratio (or thickness of the board) is increased to $\alpha = .5$, then Fig. 4 seems to indicate an increase in the thermal resistance for Bi = .01. In comparing practical problems in microelectronics packaging, though, the increase in board thickness is usually intended for fixed values of the convective heat transfer coefficients and the thermal conductivity. Thus a factor of 10 increase in thickness not only raises α from .05 to .5 but also the Biot numbers from .01 to .1.

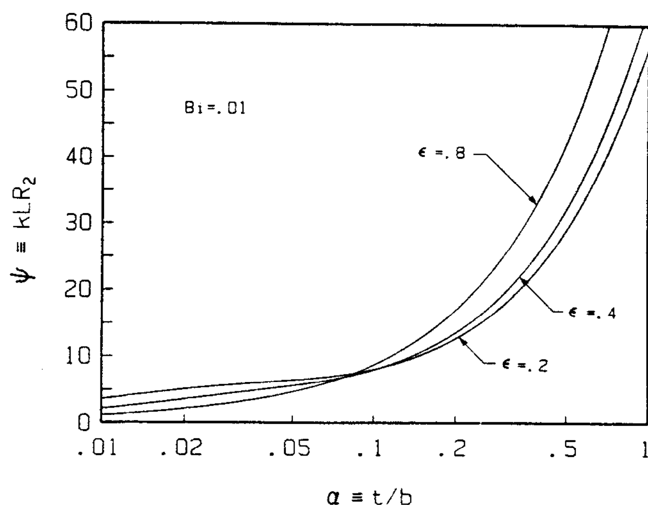

Fig. 4 Dimensionless Resistance Versus Board Aspect Ratio and Relative Contact Size for $Bi_1=Bi_2=.01$

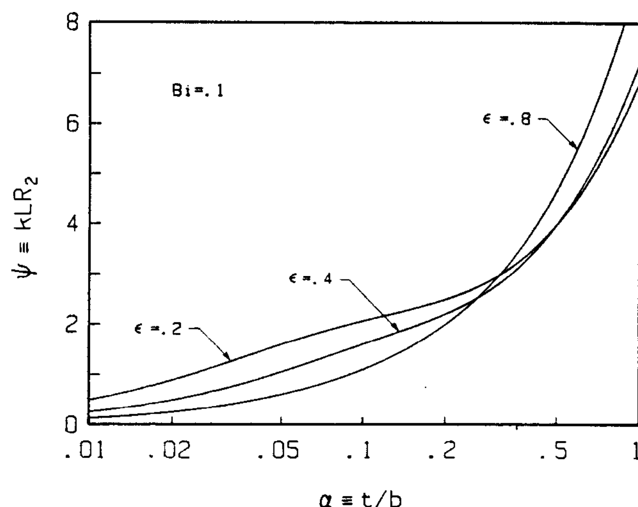

Fig. 5 Dimensionless Resistance Versus Board Aspect Ratio and Relative Contact Size for $Bi_1=Bi_2=.1$

examination of Fig. 5 now shows a decrease in thermal resistance. Similar ambiguity results with changes in ε. For example, if one wishes to investigate the effect of halving the spacing between IC chips on the board then not only will ε increase by a factor of 2 but also α for a fixed board thickness. Therefore presentation of extensive results in the form of the four dimensionless parameters is not just unfeasible but also potentially confusing.

A specific example problem is now examined to better illustrate the impact of different convective cooling and geometrical configurations on the thermal performance of a microelectronic circuit board. In this example problem an integrated circuit chip 15 mm in width is placed on a circuit board with thermal conductivity of 1 W/mK at center-to-center spacings of 20, 30, and 60 mm and heat transfer coefficients typical of both free and forced air cooling are prescribed. With reference to the basis problem illustrated in Fig. 3, the appropriate parameters are then

$a = 7.5$ mm
$k = 1$ W/mK
$b = 10, 15, 30$ mm
$5 \leq h_1 = h_2 \leq 100$ W/m^{2}K
$.5 \leq t \leq 20$ mm

With the exception of the board thickness t, these values are believed to be indicative of potential situations encountered in surface-mount packaging of integrated circuit chips. The unrealistic range board thicknesses from the very thin (.5 mm) to the extremely thick (20 mm) is considered so that a complete range of thermal responses due to the chip spacing-board thickness interaction can be illustrated. For integrated circuit chips of widths other than 15 mm and board conductivities different from k=1 W/mK, the "thin-board" or "thick-board" effects shown in this example problem may become important even for typical board thicknesses. On this note the reader is cautioned that extrapolations from the results to follow should be made very carefully. Implementation of the expressions for thermal resistance derived in this work is fairly straightforward and is encouraged so that approximate thermal optimization of microelectronic circuit boards can be accomplished on an individual case basis.

The values of the dimensionless thermal resis-

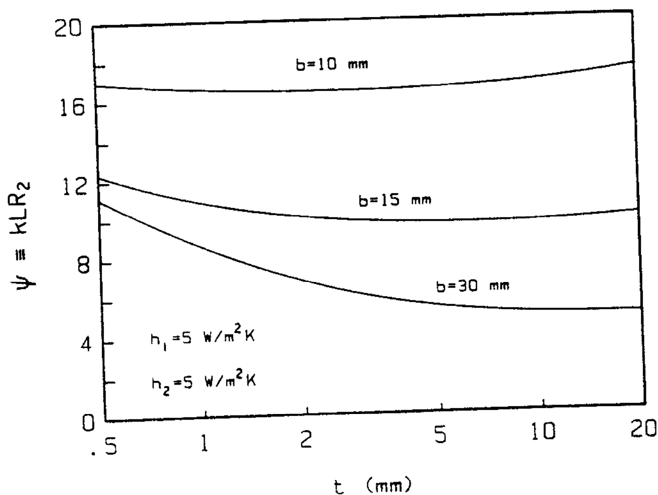

Fig. 6 Dimensionless Resistance of Example Problem for h_1=h_2=5 W/m^{2}K

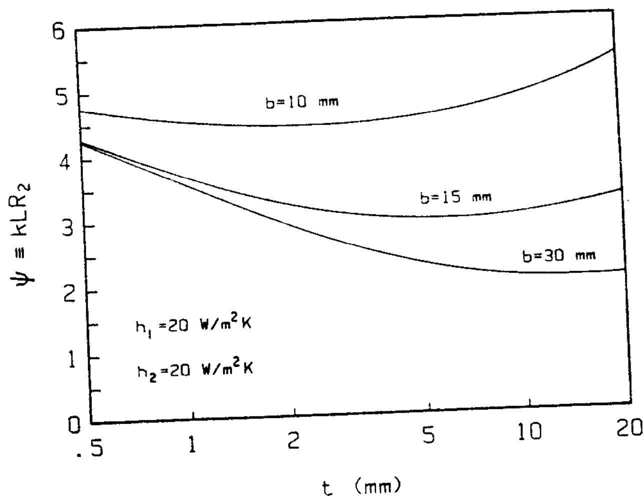

Fig. 7 Dimensionless Resistance of Example Problem for h_1=h_2=20 W/m^{2}K

tance, $\psi \equiv kLR_2$, computed for this example problem are summarized graphically in Figs. 6-9. The results for convective coefficients typical of natural convection cooling are shown in Figs. 6 and 7. For $h_1 = h_2 = 5$ W/m^{2}K, Fig. 6 shows clearly that major reductions in thermal resistance arise by increasing the chip spacing (i.e. larger b) but board thickness has little effect especially for small b(or large $\varepsilon \equiv a/b$). When $h_1 = h_2 = 20$ W/m^{2}K as shown in Fig. 7 though, the influence of board thickness is far more significant. In fact, in this situation substantial reductions in thermal resistance due to increased chip spacing are realized only when sufficiently thick boards are available to allow heat flow to the extended surface area with minimal constriction resistance. However, it is now possible to have a board which is too thick for a given chip spacing because a substantial fraction of the total heat flow exits via the bottom surface and an increased thickness also increases the solid resistance between the chip and this surface.

The results shown in Figs. 8 and 9 are more indicative of situations encountered in forced-air cooling of microelectronic circuit boards. From Fig. 8 where $h_1 = h_2 = 50$ W/m^{2}K, the effect of increased chip spacing is seen to be minimal for $b \geq 15$ mm and typical board thicknesses on the order of $t = 2$ mm. Furthermore, an "optimized" thickness for convective cooling with $h_1 = h_2$ 20 W/m^{2}K and $b = 30$ mm gives a thermal resistance nearly identical to that of $h_1 = h_2 = 50$ W/m^{2}K with $b = 30$ mm and $t = 2$ mm. When the convective heat transfer coefficients are increased to $h_1 = h_2 = 100$ W/m^{2}K as shown in Fig. 9, chip spacing has almost no effect except for very thick boards and the thinner boards are generally seen to be less resistive.

A special case which may occasionally occur, for example, due to an enclosure of the bottom surface of a microelectronic circuit board, is considered in Fig. 10. In this problem $h_1 = 50$ W/m^{2}K provides a much higher heat transfer coefficient to the top surface than that of the bottom where $h_2 = 5$ W/m^{2}K. In this case board thicknesses below some given value at each chip spacing tend to "choke-off" the heat flow

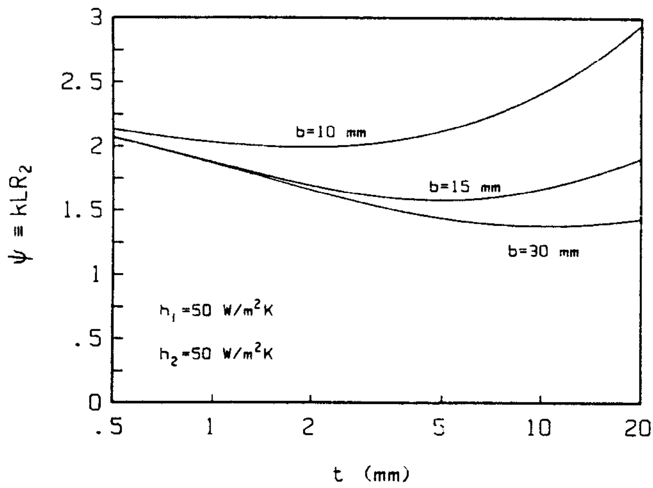

Fig. 8 Dimensionless Resistance of Example Problem for $h_1=h_2=50$ W/m^2K

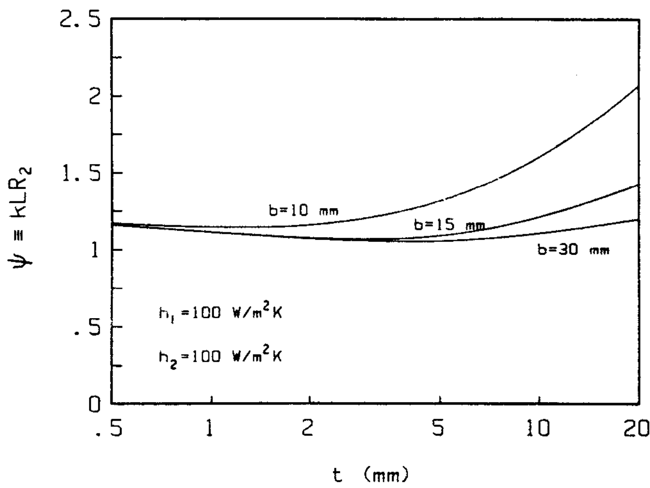

Fig. 9 Dimensionless Resistance of Example Problem for $h_1=h_2=100$ W/m^2K

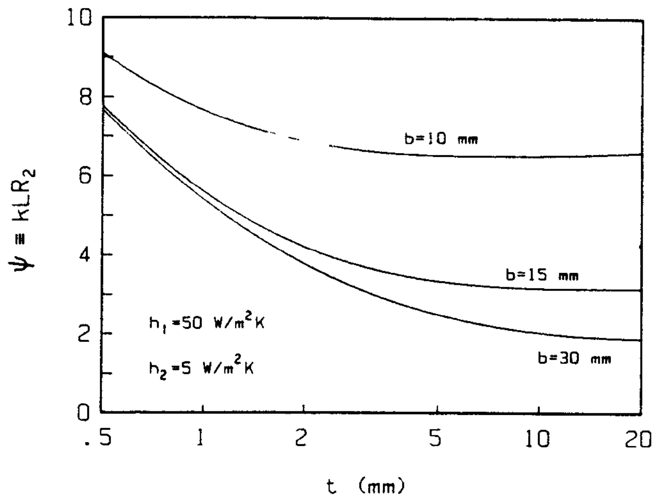

Fig. 10 Dimensionless Resistance of Example Problem for $h_1=50$ W/m^2K and $h_2=5$ W/m^2K

from the chip to the top surface of the board and thus increase the thermal resistance. Finally, Fig. 11 summarizes another special case in which the addition of a high thermal conductivity, water-cooled cold plate attached to the bottom surface of the board with negligible contact resistance is simulated. For this situation it is desirable to keep the board as thin as possible and chip spacing has almost no effect. This allows dense packaging of integrated circuit chips to be used with little thermal penalty.

The relative importance of convective cooling by the heat flow path through the bottom surface of the integrated circuit chip can be illustrated by considering the effective heat transfer coefficients on the top and bottom surfaces ofthe chip, or h_{e1} and h_{e2} respectively. The heat transfer coefficient on the top surface of the chip can be approximated as being the same as that on the top surface of the circuit board, or

$$h_{e1} \approx h_1 \tag{33}$$

The bottom coefficient h_{e2} can be found by interpreting the thermal resistance R_2 as an effective heat transfer coefficient on the bottom surface of the integrated circuit chip, or

$$h_{e2} \approx \frac{k}{\psi a} \tag{34}$$

By using values of ψ computed for the example problem where $a = 7.5$ mm and $k = 1$ W/m K, comparitive values of h_{e1} and h_{e2} have been compiled in Table i for a variety of convective coefficients h_1 and h_2 and chip spacings b. Note that a board thickness of $t = 2$ mm is assumed for all results shown in Table 1. Note further that the values of h_{e1} reported in Table 1 are probably too low relative to h_1 and h_2 as the work of Culham (1985) shows that heat transfer coefficients on a chip are usually around 50% higher than that of the top surface of the circuit board. In addition the values of h_{e2} reported in Table 1 are probably too high relative to h_1 and h_2 due to the neglect of contact resistance between the integrated circuit chip and the circuit board. Nonetheless, the

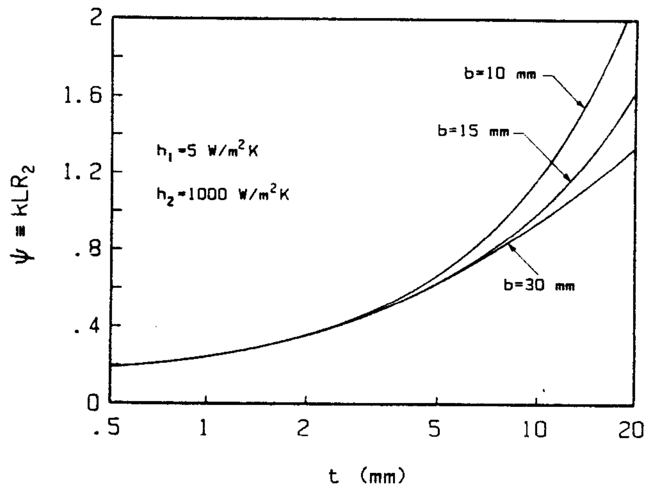

Fig. 11 Dimensionless Resistance of Example Problem for $h_1=5$ W/m^2K and $h_2=1000$ W/m^2K

h_1 (W/m^2K)	h_2 (W/m^2K)	b (mm)	h_{e1} (W/m^2K)	h_{e2} (W/m^2K)
5	5	10	5	8.1
		15		13.3
		30		19.6
20	20	10	20	30.2
		15		41.4
		30		45.8
50	50	10	50	67.0
		15		78.9
		30		80.7
100	100	10	100	115
		15		124
		30		125
50	5	10	50	19.4
		15		31.2
		30		35.3
5	1000	10	5	371
		15		373
		30		373

Table 1. Effective heat transfer coefficients for an integrated circuit chip with a = 7.5 mm, k = 1 W/mK, and t = 2 mm.

results in Table 1 still indicate clearly that a significant portion of the total heat flow from an integrated circuit chip can exit via the bottom heat flow path Q_2 in Fig. 2 for practical applications with surface-mount packaging. Thus analysis and optimization of the heat flow path into the circuit board is seen to be an important step towards a final goal of allowing maximum power density for a given maximum device operating temperature with minimum cost.

A ONE-DIMENSIONAL MODEL: THE COMPOUND-FIN

As mentioned previously, an accurate prediction of the thermal performance of microelectronic circuit boards really requires consideration of the interaction between the thermal-fluid boundary layer and heat conduction in the circuit board. To achieve this goal with a minimum of computational effort, Culham (1985) has coupled a boundary layer analysis with a one-dimensional heat conduction model, the compound-fin. In this approximate heat conduction model the temperature is assumed to vary only along the length of the board, or T=T(x) only in Fig. 3. Physically, this approximation indicates that temperature changes in the x-direction of Fig. 3 are much greater than those in the z-direction or that the temperature drop in the z-direction of the solid is much less than the temperature drop across the thermal boundary layer.

In a compound-fin approximation, the prescribed heat flux and convective cooling on the top and bottom surfaces of the fundamental basis problem shown in Fig. 3 are modelled as sources and sinks respectively in a one-dimensional heat balance equation. By solving the simple constant-coefficient ordinary differential equation which results and applying the boundary conditions of adiabatic ends at x = 0 and x = b, the dimensionless thermal resistance of the compound-fin approximation of Fig. 3 can easily be derived as

$$\psi_{CF} = \frac{\alpha}{\varepsilon}\left\{\frac{1}{Bi_2} + \frac{C_1}{m_1\varepsilon}\left(e^{m_1\varepsilon} - e^{-m_1\varepsilon}\right)\right\} \quad (35)$$

where $$m_1 \equiv \sqrt{Bi_2}\,/\alpha \quad (36)$$

$$m_2 \equiv \sqrt{Bi_1 + Bi_2}\,/\alpha \quad (37)$$

and $$C_1 = \frac{1/Bi_2}{\frac{m_1\sigma_1}{m_2}\left(e^{m_2(\varepsilon-2)} + e^{-m_2\varepsilon}\right) - e^{-m_1\varepsilon} - e^{m_1\varepsilon}} \quad (38)$$

$$\sigma_1 = \frac{e^{m_1\varepsilon} - e^{-m_1\varepsilon}}{e^{m_2(\varepsilon-2)} - e^{-m_2\varepsilon}} \quad (39)$$

These expressions are not valid when the bottom surface is insulated, or $Bi_2 \approx 0$. In this case a similar one-dimensional analysis can show that

$$\psi_{CF}(Bi_2{=}0) = C_2\frac{\alpha}{\varepsilon} - \frac{\varepsilon}{6\alpha} \quad (40)$$

where $$C_2 = C_3\left(e^{-m_2\varepsilon} + e^{m_2(\varepsilon-2)}\right) + \varepsilon^2/2\alpha^2 \quad (41)$$

$$C_3 = \varepsilon/m_2\alpha^2\left(e^{-m_2\varepsilon} - e^{m_2(\varepsilon-2)}\right) \quad (42)$$

In Fig. 12 the ratio of the compound-fin resistance to the exact two-dimen-sional resistance, ψ_{CF}/ψ, is plotted against $Bi{=}Bi_1{=}Bi_2$ for the case of ε=.5 and α=.2. Examination of extensive numerical results has shown that errors in ψ_{CF} relative to ψ of Eq. (31) generally decrease as ε increases and α decreases. Furthermore when $Bi_1 \neq Bi_2$ the error in ψ_{CF} is usually less than that shown in Fig. 12 for Bi=max (Bi_1, Bi_2).

From Fig. 12 the compound-fin model is found to underpredict the true thermal resistance. This is expected since its derivation assumes that internal solid resistances are small relative to film resistances and thus neglects their contribution. The relative error in ψ_{CF} for the case shown in Fig. 12 is generally on the order of the Biot number for Bi $\leq$ .5. Therefore, if errors in resistance greater than 10% are not tolerable, then the one-dimensional approximation given by the compound-fin model is of limited utility for Bi > .1. In fact, the actual surface temperatures (which are required in a model that couples heat conduction and boundary-layer analyses) may be significantly more in error for a given Biot number than the resistance which is based on an average temperature.

Physically the Biot number should reflect the

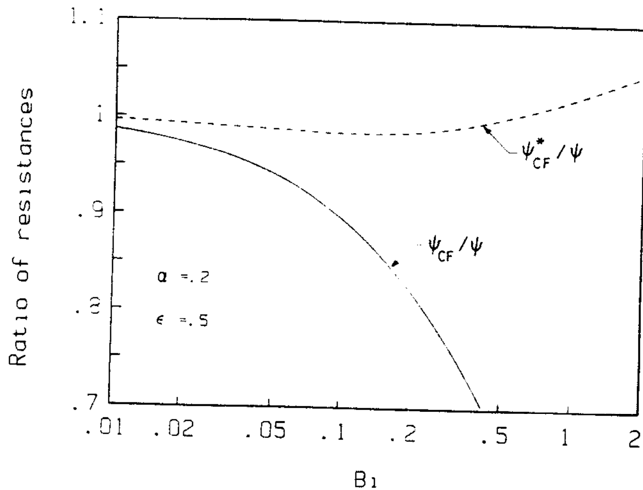

Fig. 12 Ratio of 1-D to 2-D Resistances for the Compound-Fin Model (ψ_{CF}/ψ) and the Modified Compound-Fin Model (ψ^*_{CF}/ψ) Versus Biot Number B_i for top and bottom surfaces

ratio of the solid resistance, R_s, to the fluid-film resistance, R_f, in a system or $Bi \approx R_s/R_f$. For "small" Biot numbers one might approximate the total thermal resistance, R_t, as the sum of the solid and fluid-film resistances acting in series, or

$$R_t \approx R_s + R_f \approx R_f(1 + Bi)$$

which suggests that a better estimation of the thermal resistance of the basis problem of Fig. 3 can be made using a compound-fin model if the factor (1+Bi) is applied to ψ_{CF} to give

$$\psi^*_{CF} \equiv \psi_{CF}(1+Bi) \qquad (43)$$

A plot of ψ^*_{CF}/ψ is also shown in Fig. 12 and the increase in accuracy of this "modified" compound-fin model is substantial. Thus an important future improvement to the compound-fin model would be the development of similar correction factors which can better estimate actual surface temperatures while still using only a one-dimensional heat conduction model.

CONCLUSIONS

In this work an approximate model to predict the thermal resistance of convectively-cooled microelectronic circuit boards has been developed by considering a fundamental basis problem for heat conduction in the board. An approximate analytical solution to this basis problem which can provide any desired accuracy was derived by employing a novel approach for treating mixed boundary conditions. An individual problem of this type could be readily solved using standard numerical methods. However this approximate solution allows interactive evaluations of the thermal advantages or disadvantages for different circuit board configurations or convective cooling arrangements to be made rapidly on a personal computer.

The results obtained for a practical example problem indicate that either a "thin" or "thick" circuit board can be desirable depending on the interaction of the different variables which contribute to the thermal resistance. In particular, a decrease in the thermal resistance of the board due to increased chip spacing often occurs only when accompanied by a similar increase in the board thickness (which is often not feasible). Thus increasing the chip center-to-center spacing to a distance greater than twice the chip width normally produces little benefit in decreased thermal resistance for the penalty of decreased packaging density except when the convective coefficients are fairly low (i.e. free convection). In some cases where the convective heat transfer coefficients are very high, it is desirable to make the board as thin as possible and the integrated circuit chips can be placed close together without increasing the thermal resistance of the circuit board.

Finally, the accuracy of the compound-fin model for one-dimensional steady heat conduction in a microelectronic circuit board has also been investigated. The compound-fin model underpredicts the actual thermal resistance with a relative error generally exceeding 10% for Bi > .1 where Bi is the maximum of the top and bottom surface Biot numbers. A substantial increase in the accuracy of the compound-fin model was observed when a simple correction factor derived from physical considerations was applied.

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APPENDIX I

The solution of Eq. (24) for the series coefficients A_n requires the evaluation of the matrix coefficients C_{mn} and G_n. The coefficients C_{mn} are determined by exact integration of Eq. (25) to give

$$C_{mn} = \Delta_{mn} \gamma_3^2(1 - \delta_{mn})[n\pi\alpha\Omega_n + m\pi\alpha\Omega_m + Bi_1]$$

$$+ \delta_{mn}[(n\pi\Omega_n\alpha\gamma_3)^2/2 + \tau_n\gamma_3(2\gamma_3\pi\alpha\Omega_n + Bi_1)]$$

$$+ \Lambda_n\Lambda_m[2\gamma_4 Bi_1(1 - \varepsilon) + \gamma_4^2 + Bi_1^2(1 - \varepsilon) - n\pi\Omega_n\alpha\gamma_3$$

$$- m\pi\Omega_m\alpha\gamma_3 - 2\gamma_3(\gamma_4 + Bi_1)] \qquad \text{(A-1)}$$

where δ_{mn} is the familiar Kronecker delta function, Ω_n, Λ_n, and γ_3 are defined by Eqs. (11), (13) and (14) respectively, and

$$\Delta_{mn} = (-Bi_1/2)[\frac{\sin(n-m)\pi\varepsilon}{(n-m)\pi} + \frac{\sin(n+m)\pi\varepsilon}{(n+m)\pi}] \qquad \text{(A-2)}$$

$$\tau_n = Bi_1[(1 - \varepsilon)/2 - \frac{\sin 2n\pi\varepsilon}{4n\pi}] \qquad \text{(A-3)}$$

$$\gamma_4 = Bi_2/Bi_2 + 1 \qquad \text{(A-4)}$$

The coefficients G_n are determined similarly by exact integration of Eq. (26) to give

$$G_n = \gamma_3^2\,\Omega_n\alpha \sin n\pi\varepsilon +$$

$$\varepsilon\Lambda_n[Bi_3^2(1 - \varepsilon) - \gamma_4^2 - \gamma_3\,(Bi_1 + n\pi\Omega_n\alpha)] \qquad \text{(A-5)}$$